Semiconductor Electronics: Materials, Devices and Simple Circuits

14

INTRODUCTION

Electronics - Electron's dynamics

The word "electronics' is derived from electron + dynamics which means the study of the behavior of an electron under different conditions of externally applied fields.

That field of science which deals with electron devices and their utilization. "Here an electronic device is "a device in which conduction takes place by the movement of electron - through a vacuum, a gas, or a semiconductor. Some familiar devices are

(1) Rectifier (2) Amplifier (3) Oscillator etc.

Important point :

* Main application of electronics is computer which is used in every field.
* All electronics equipment required D.C. supply for operation (not A.C. supply)

Classification of Electronics (According to Technology)	
Vacuum tube electronics	**Semiconductor electronics**
Both technology based on behavior of electron	
Electron	
Bonded electron	**Free electron**
(1) Revolve around nucleus and bounded by attraction force of nucleus.	(1) Freely move in substance, there is almost no attraction of nucleus.
(2) Can't help in flow of current	(2) Help in flow of current.
(3) All electrons have different properties.	(3) All electrons have same properties.

ENERGY BANDS IN SOLIDS

Based on - Pauli's exclusion principle

In an Isolated atom electrons present in energy level but in solid atoms they are not isolated there is interaction among each other due to this energy level splited into different energy level Quantity of these different energy level depends on quantity of interacting atom. Splitting of sharp and closely compact energy level results energy band. This is de create in nature. Order of energy levels in a band is 10^{23} and their energy difference = 10^{-23} eV.

1. SOME IMPORTANT DEFINITIONS

(1) Energy Band - Range of energy possessed by electron in a solid is known as energy band.

(2) Valence Band (VB) - Range of energies possessed by valence electron is known as valence band,

(a) Have bonded electron

(b) No flow of current due to such electron

(c) Always fulfill by electron

(3) Conduction Band (CB)

Range of energies possessed by free electron is known as conduction band.

(a) Also called empty band of minimum energy.

(b) In general Partialy filled by electron.

(c) If Conduction Band is empty, then conduction is not possible.

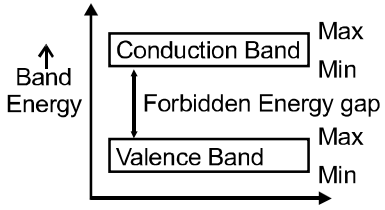
(4) Forbidden Energy gap (FEG) (ΔEg) -

[Δ Eg. = $(C B)_{Min}$ - $(V B)_{Max}$]

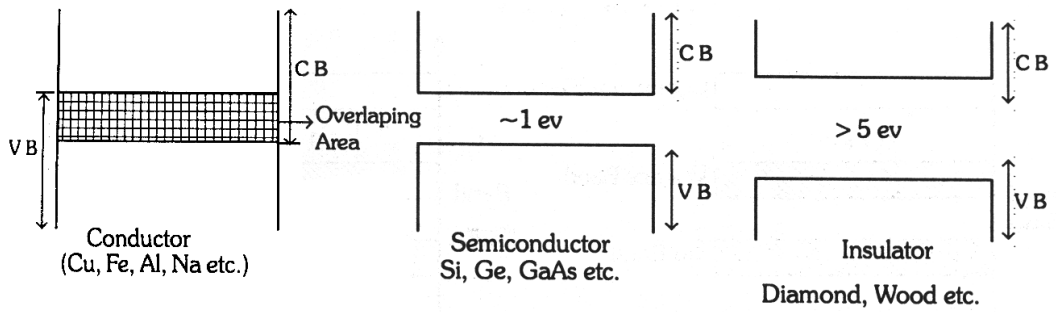
Energy gap between conduction band and valence band, where no free electrons exist.

Special Points :

* No free electron present in F.E.G.
* Width of F.E.G. depends upon the nature of substance.
* Width is more, then valence electrons are strongly attached with nucleus
* Width of F.E.G. is represented in eV.
* As temp ↑ F.E.G. ↓ (Very slightly)



According to Energy Band Theory: Explanation of Conductor, Semiconductor & Insulator.



CONDUCTOR :

In some solids conduction band and valence band are overlapping there is no any band gap, between them it means ΔE_g =,0. Due to this a large number of electrons available for electrical conduction and therefore its resistivity is low ($\rho = 10^{-2} - 10^{-8}$ ΩM) and conductivity is high ($\sigma = 10^2 - 10^8$ mho/m). Such material called conductor. For **example** gold, silver, copper etc.

INSULATOR :

In some solids energy gap is large (Eg > 3 eV). So in conduction band there are no electrons and so no electrical conduction is possible. Here energy gap is so large that electrons cannot be easily excited from the valence band to conduction band by any external energy (electrical, thermal or optical). Such material called as "insulator"; Its $\rho = 10^8$ Ω–m & $\sigma = 10^{-8}$ $(\Omega\text{-m})^{-1} = 10^{-8}$ Sm^{-1}

SEMICONDUCTOR :

In some solid a finite but small bandgap (Eg < 3eV) exists. Due to this small band gap some electrons can be thermally excited to "Conduction band". These thermally excited electron can move in conduction band and can conduct current their resistivity and conductivity both are in medium range. its $\rho = 10^5 - 10^0$ Ω-m & $\sigma = 10^{-5} - 10^0$ Sm^{-1}

Example of Semiconductor Material

Elemental semiconductor = Si and Ge

Compound Semiconductor,

Inorganic = CdS, GaAs, CdSe, InP etc.

Organic = anthracene, doped phalocyanines.

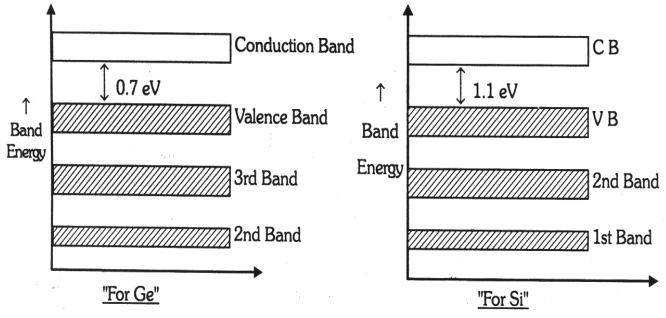
Organic polymers = Poly pyrrole, Poly aniline, polythiophene etc.

PROPERTIES OF SEMICONDUCTORS

* Negative temperature coefficient (a), T ↑, R ↓ ρ↓, σ↑, I↑
* Covalent Bond
* Crystalline structure [Face centred cubic (FCC)]
* By adding small impurity conduction properties change.
* Place in Periodic Table → IV group
* Forbidden Energy gap (0.1 to 3 eV)
* There are many semiconductor but few of them have practical application in electronics like

Ge & Si Ge → 32 2, 8, 18, 4

Si → 14 2, 8, 4



8. Charge Carriers

(i) Electron (ii) Hole

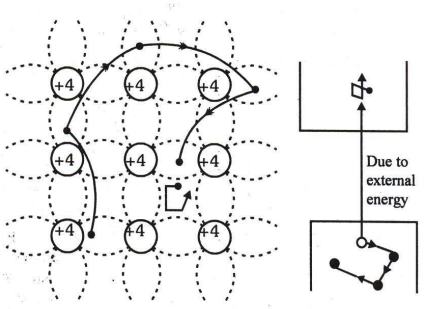
CONCEPT OF "HOLES" IN SEMICONDUCTORS

Due to external energy (temp. or radiation) when electron goes from valence band to conduction band (i.e. bonded electrons becomes free), vacancy of free e^- create in VB.

Which have same charge as electron but positive, this positively charged vacancy which move randomly. In semiconductor solid it is shown in diagram called as hole.

This positively charged randomly moved electron vacancy called as"**hole**"

1. Missing electron in VB.
2. It acts as +ve charge.
3. Effective mass is more than electron.
4. Mobility of hole is less than electron



Note: *hole acts as virtual charge, although there is no physical charge on it.*

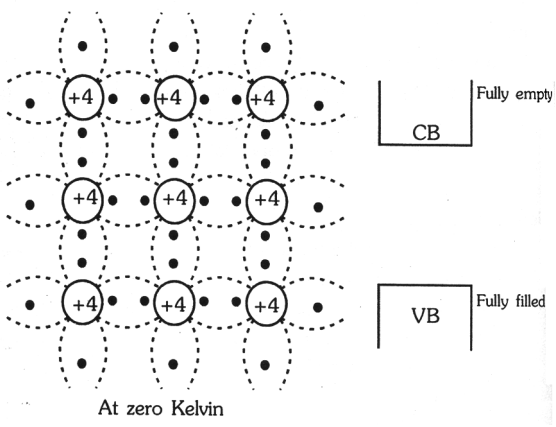
HOLE CURRENT

At room temp, due to breaking of some Covalent Bonds some free electrons are produced. By applying electric field current flow due to free electrons. At same time hole current also flow in semiconductor.

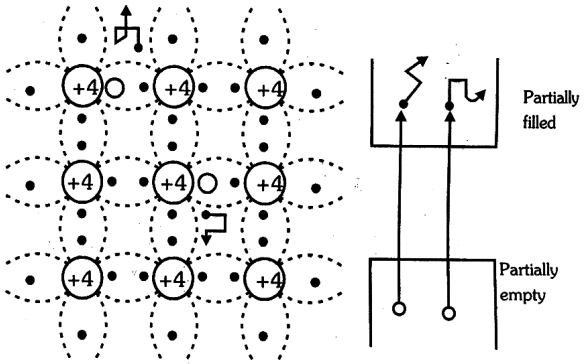
EFFECTING FACTOR

I. EFFECT OF TEMPERATURE :

1. **At absolute zero kelvin temp.** : At this temp Covalent Bonds are very strong and there are no free electron and semiconductor behaves as perfect insulator



2. **Above absolute temp. :** When temp increases some of Covalent Bonds are break due to thermal Energy supplied. These free electron can constitute a tiny electric current if potential difference is applied accross semiconductor crystal. This shows that R↓. by T↑ so (-ve α)



Important point

* No. of Electrons reaching from VB to CB

  $n = A\,T^{3/2}\; e^{-\frac{\Delta Eg}{2kT}}$

  k = Boltzmann Const = 1.38×10^{-23} J/k

  T = Absolute Temp.

  A = Simple constant
* For Silicon solid at room temperature out of approximate 10^{12} silicon atoms only one electron goes from VB to CB.
* For Germanium solid at room temperature out of approximate 10^{9} germanium atoms only one electron goes from VB to CB.
* In semiconductors, Ohms law is obeyed only for low electric field (less than 10^{6} Vm^{-1}). Above this field, the current becomes almost independent of applied field.

ii. Effect of impurity in semiconductor

Doping is a method of addition of "desirable" impurity atoms to pure semiconductor to increase **conductivity** of semiconductor.

Important point

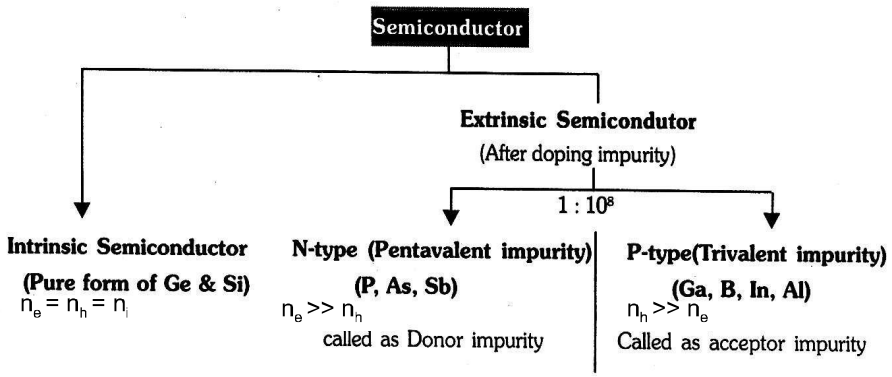
* The concentration of dopant atoms be very low, doping ratio is vary from

  impure: pure :: 1 : 10^{6} to 1 : 10^{10}

  In general it is 1 : 10^{8}
* There are two main method of doping.

  (i) Alloy method (ii) Diffusion method (The best)
* The size of dopant atom (impurity) should be almost the same as that of crystal atom. So that crystalline structure of solid remain unchanged.

CLASSIFICATION OF SEMICONDUCTOR

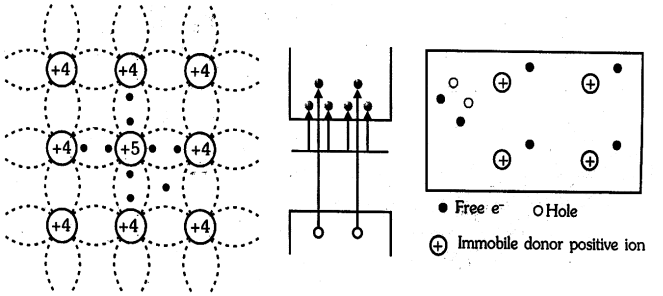


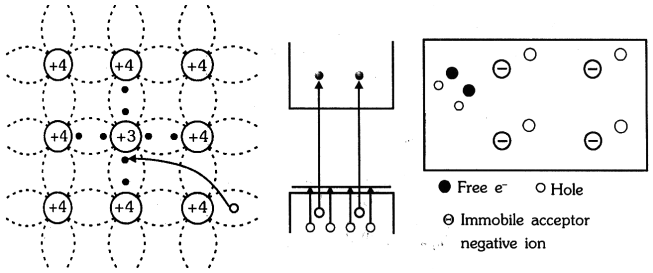
N TYPE SEMICONDUCTOR:

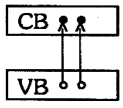
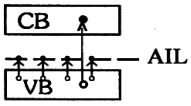
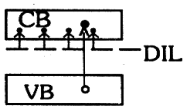
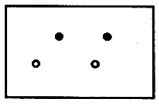
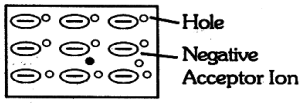
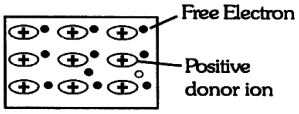
When a pure semiconductor (Si or Ge) is doped by pentavalent impurity (P, As, Sb, Bi) then four electrons out of the five valence electrons of impurity take part, in covalent bonding, with four silicon atoms surrounding it and the fifth electron is set free. These impurity atoms which donate free e- for conduction are called Donor impurity (N_D). Here free e-increases very much so it is called as "N" type semiconductor here impurity ions are known as "Immobile Donor positive Ion". "Free e^-" called as "majority" charge carries and "holes" called as "minority" charge carriers.

P TYPE SEMICONDUCTOR :

When a pure semiconductor (Si or Ge) is doped by trivalent impurity (B, AI, In, Ga) then outer most three electrons of the valence band of impurity take part, in covalent bonding with four silicon atoms surrounding it and except one electron from semiconductor and make hole in semiconductor. These impurity atoms which except bonded e- from valance band are called as Acceptor impurity (N_A). Here holes increases very much so it is called as "P" type semiconductor here impurity ions known as "Immobile Acceptor negative Ion". Free e^- called as minority charge carriers and holes called as majority charge carriers.





1.			
2.			
3.	Current due to electron & Hole	Mainly due to holes	Mainly due to electrons
4.	$n_e = n_h = n_i$	$n_h >> n_e$ ($N_A \simeq n_h$)	$n_h << n_e$ ($N_D \simeq n_e$)
5.	$I = I_e + I_h$	$I \simeq I_h$	$I \simeq I_e$
6.	Entirely Neutral	Entirely Neutral	Entirely Neutral
7.	Quantity of Electrons & Holes are equal	Majority - Holes Minority - Electrons	Majority - Electrons Minority - Holes

Mass action Law : In any semiconductor due to thermal effect, generation of free e^- and hole take place. A part from the process of generation, a process of recombination also occurs simultaneously. In which free e^- further recombine with hole. At equilibrium rate of generation of charge carries u equal to rate of recombination of charge carrier.

The recombination occurs due to e- colliding with a hole, larger value of n_e or n_h, higher is the probability~ of their recombination.

Hence for an extrinsic rate of recombination $\alpha\, n_e \times n_h$ .....(1)

so rate of recombination = $Kn_e \times n_h$

Here, K is recombination coefficient, for intrinsic semiconductor $n_e = n_h = n_i$

Rate of recombination = Kn_i^2

.....(2)

The value of K remain constant for a solid, according to law of thermodynamics until crystalline lattice structure remain same so

$Kn_e \times n_b = Kn_i^2$

$$\boxed{Kn_i^2 = n_i^2 = n_e \times n_h}$$

Important point

Under thermal equilibrium, the product of the concentration 'n_e' of free electrons & the concentration n_h of holes is a constant, independent of the amount of doping by acceptor & donor impurities.

Mathematically n_e x $n_h = n_i^2$

Mass action law

Solved Examples

Ex.1 The energy of a photon of sodium light (λ = 589 nm) equals the band gap of a semiconducting material.

(a) Find the minimum energy E required to create a hole-electron pair.

(b) Find the value of E/kT at a temperature of 300 K

Sol. (a) $E = h\nu = \frac{hc}{\lambda}$ (in J) $= \frac{hc}{e\lambda}$ (in eV),

So $E = \frac{12400}{\lambda}$

Here E is in eV and λ is in Å

λ = 589 nm = 5890 Å

$E = \frac{12400}{5890} = 2.1$ eV

(b) $\frac{E}{kT} = \frac{2.1 \text{ (eV)}}{1.38\times10^{-23}\times300\text{(J)}}$,

$\frac{E}{kT} = \frac{2.1\times1.6\times10^{-19}\text{J}}{1.38\times10^{-23}\times300\text{(J)}} = 81$

Ex.2 A P type semiconductor has acceptor level 57 meV above the valence band What is maximum wavelength of light required to create a hole ?

Sol. $E = \frac{hc}{\lambda}\text{(in J)} = \frac{hc}{e\lambda}\text{(in eV)}$

$= \frac{6.62\times10^{-34}\times3\times10^{8}}{57\times10^{-3}\times1.6\times10^{-19}} = 217100\,\text{Å}$

Ex.3 A silicon specimen is made into a p-type semiconductor by doping on an average one indium atom per 5 x 10^7 silicon atoms. If the number density of atoms in the silicon specimen is 5 x 10^{28} atoms/m^3 ; find the number of acceptor atoms in silicon per cubic centimeter.

Sol. The doping of one indium atom in silicon semiconductor will produce one acceptor atom in p-type semiconductor. Since one indium atom has been dopped per 5×10^7 silicon atoms, so number density of acceptor atoms in silicon

$\frac{5\times10^{28}}{5\times10^{7}} = 10^{21}$ atoms/m^3 = 10^{15} atoms/cm^3

Ex.4 The concentration of hole - electron pairs in pure silicon at T = 300 K is 7 x 10^{15} per cubic meter. Antimony is doped into silicon in a proportion of 1 atom in 10^7 Si atoms. Assuming that half of the impurity atoms contribute electron In the conduction band, calculate the factor by which the number of charge carriers in creases due to doping the number of silicon atoms per cubic metre is 5×10^{28}.

Sol. In pure semiconductor

electron-hole pair = 7 x 10^{15}

$n_{\text{total initial}} = n_h + n_e = 14 \times 10^{15}$

after doping :

Donor impurity,

$N_D = \frac{5\times10^{28}}{10^{7}} = 5\times10^{21}$

According to question

$n_e = \frac{N_D}{2} = 2.5\times10^{21}$

so $n_{\text{final}} = n_h + n_e$

Here $n_e >> n_h$

so $n_{\text{final}} \approx n_e \approx 2.5 \times 10^{21}$

Factor = $\frac{n_{\text{final}} - n_{\text{initial}}}{n_{\text{initial}}} \approx \frac{2.5\times10^{21}}{14\times10^{15}} = 1.8\times10^{5}$

RESISTIVITY AND CONDUCTIVITY OF SEMICONDUCTOR

Conduction in conductor

a. Relation between current (I)

& drift velocity (V_D)

$I = ne\ A\ V_d$

n = No. of electron in unit volume

$J = neV_d$

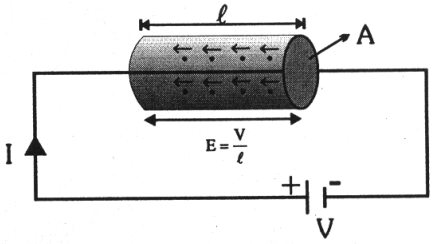
A = cross sectional Area

$J = ne\ \mu E$

V_d = Drift velocity of electron = μE

$J = \sigma E$ $\quad J = \frac{I}{A}$ Amp/m^2 current density

$\sigma = ne\mu = 1/\rho$ $\quad \sigma$ = conductivity $\quad \rho$ = Resistivity



Mobility $\mu = \frac{V_d}{E}$ $\quad \mu$ = Mobility

Conduction in Semiconductor -

Intrinsic semiconductor	**p-type**	**N-type**
$n_e = n_h$	$n_h >> n_e$	$n_e >> n_h$
$J = ne\ [v_e + v_h]$	$J \cong en_h v_h$	$J \cong e\ n_e\ v_e$
$\sigma = \frac{1}{\rho} = en[\mu_e + \mu_h]$	$\sigma = \frac{1}{\rho} \cong en_h\ \mu_h$	$\sigma = \frac{1}{\rho} \cong en_e\ \mu_e$

Important point

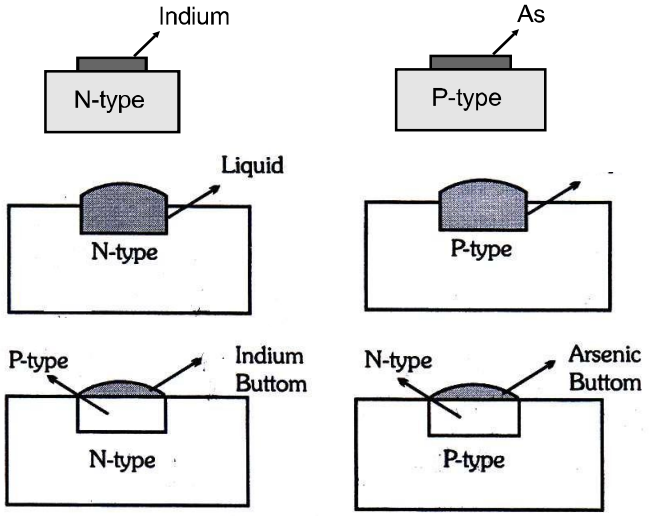
* Due to impurity the conductivity increases approx 10^3 times
* $\sigma_{sc} = \sigma_e + \sigma_h = n_e e\mu_e + n_h e\mu_h$

P-N JUNCTION

Techniques for making PN Junction -

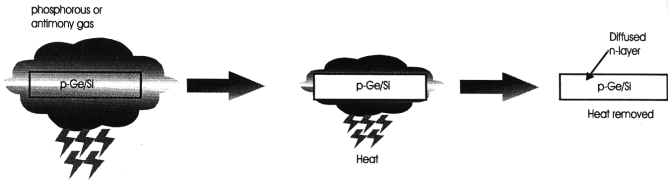
Alloy Method

Alloy Junction : Here a small piece of III group impurity like medium is placed over n-Ge or n-Si and melted as shown in figure ultimately P-N junction form.



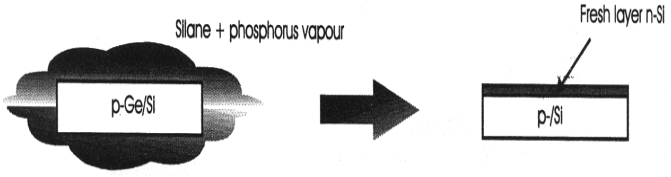
DIFFUSION JUNCTION :

A heated P-type semiconductor is kept in pentavalent impurity vapours which diffuse into P-type semiconductor as shown and make P-N junction.



VAPOUR DEPOSITED JUNCTION OR EPITAXIAL JUNCTION :

If we want to grow a layer of n-Si or p-Si then p-Si wafer is kept in an atmosphere of Silane (a silicon compound which dissociates into Si at high temperatures) plus phosphorous vapours. On creaking of silane at high temperature a fresh layer on n-Si grows 'on p-Si giving -the "P-N junction". Since this junction growth is layer by so it is also referred as layer growth or epitaxial junction formation of P-N junction.



1. DESCRIPTION OF P-N JUNCTION WITHOUT APPLIED VOLTAGE OR BIAS :

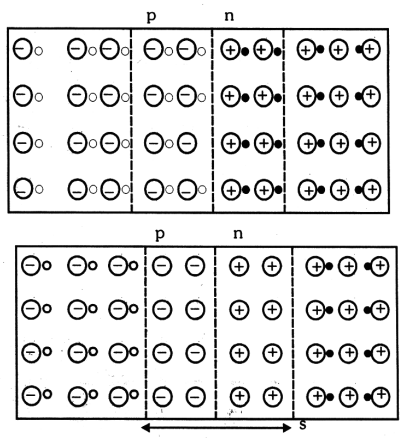
Given diagram shows a P-N junction immediately after it is formed.

P region has mobile majority holes and immobile negatively charged impurity ions.

N region has mobile majority free electrons and immobile positively charged impurity ions.

Due to concentration difference diffusion of holes starts from P to N side and diffusion of e^-s starts N to P side.

Due to this a layer of only positive (in N side) and negative (in P-side) started to form which generate an electric field (N to P side) which oppose diffusion process, during diffusion magnitude of electric field increases due to this diffusion it gradually decreased and ultimately stopped.



The layer of immobile positive and negative ions, which have no any free electrons and holes called as depletion layer as shown in diagram.

Important Point:

* **Width of depletion layer $\cong 10^{-6}$ m**

(a) As doping increases depletion layer decreases

(b) As temperature increased depletion layer also increases.

(c) P-N Jn $\rightarrow$ unohmic

* Potential Barrier

Ge $\longrightarrow$ 0.3V Si $\longrightarrow$ 0.7V

* Electric field is produced due to potential barrier

$E = V/d = 0.5 / 10^{-6} \Rightarrow E \cong 10^5$ V/m

This field prevents the respective majority carrier from crossing barrier region

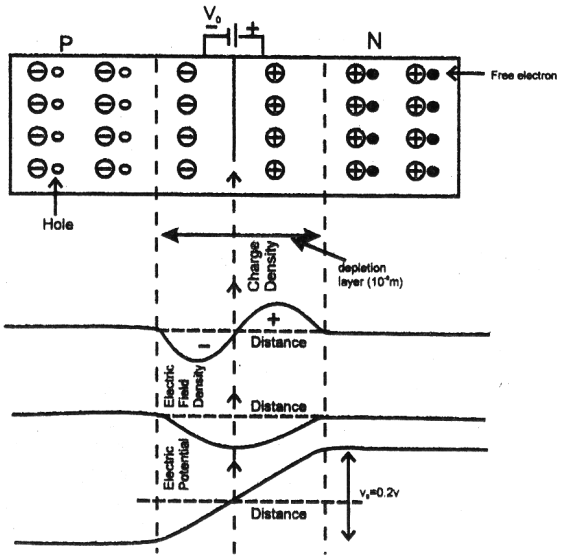
Diffusion & Drift Current

(1) Diffusion current - P to N side

(2) Drift current - N to P side

If there is no biasing diffusion current = drift current

So total current is zero



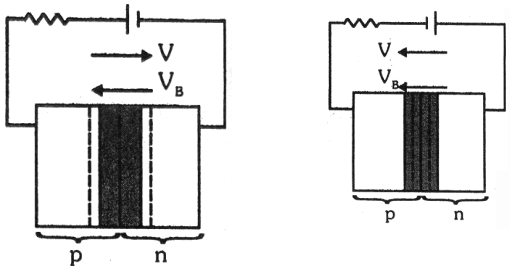
Behaviour of P-N Junction with an external voltage applied or Bias

(i) Forward Bias : If we apply a, voltage 'V" such that P-side is positive and N-side is negative as shown in diagram.

The applied voltage is opposite to the junction barrier potential. Due to this effective potential barrier decreases junction width also decreases, so more majority carrier. will be allowed to flow across junction. It means the current flow in principally due to majority charge carriers and is large (mA) called as forward Bias.

(ii) Reverse Bias : If we apply a voltage "V" such that P-side is negative and N-side is positive as shown in diagram.

The applied voltage is same side of to the junction barrier potential. Due to this effective potential barrier increased junction width also increased, so no majority carriers will be allowed to flow across junction. Only minority carriers will drifted. It means the current flow in principally due to minority charge carriers and is very small (μA) called as reversed high Bias.



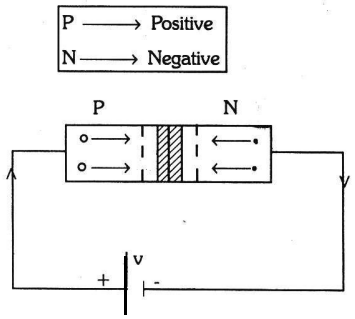
Important Points

* In reverse bias, the current is very small and nearly constant with bias (termed as reverse saturation current). However interesting behaviors results in some special cases if the reverse bias is increased further beyond a certain limit above particular high voltage breakdown of depletion layer started.
* This breakdown due to covalent breaking of deption layer termed as Zener breakdown (After the discover, C. Zener) and such a diode is Zener diode.
* Zener diodes with different breakdown voltages (for regulations of different voltages) can obtained by changing the doping concentration of its p-and n-sides.
* There is another variant of Zener like breakdown if the doping concentrations of p-and n-sides are not as high as for the case of zener diode. Such diodes will have relatively wider junction widths. At very high reverse bias, already existing electrons and holes are accelerated in the junction field and may undergo many collisions with the atoms in the crystal.
* These new electron-hole pairs are created by impact ionisation also get accelerated in the junction field and collide further with the crystal atoms giving an increasing number of new electrons and holes. These bias beyond a certain critical value. This phenomenon is known as Avalanche breakdown and the device is referred to as Avelanche diode.

Zener Break down	Avelanche Break down
Where covalent bonds of depletion layer, its self break, due to high electric field of very high Reverse bias voltage.	Here covalent bonds of depletion layers are bro ken by collision of "Minorities" which aquire high kinetic energy from high electric field of very-very high reverse bias voltage.
This phenomena predominant (1) At lower voltage after "break down" (2) P - N Jn. having "High doping"; (3) P - N Jn. having thin depletion layer Here P - N not damage permanently "In D.C voltage stablizer zener phenomena of it is sused".	This phenomena predominant (1) At high voltage after breakdown (2) P - N Jn. having "Low doping" (3) P - N Jn. having thick depletion layers Here P - N damage permanently due to' "Heating effect" due to abruptly increment minorities during repetitive collisions.

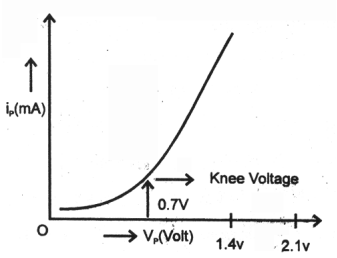
DIFFERENCE BETWEEN FORWARD BIAS & REVERSE BIAS

Forward Bias



Important point

1. Potential Barrier reduces
2. Width of depletion layer decrease
3. P-N JN provide very small resistance
4. Forward current flow in circuit
5. Order of forward current in mili amp.
6. Mainly flow majority current.
7. Forward characteristic curves.
8. Forward resistance



$$R_f = \frac{\Delta V_f}{\Delta I_f} \cong 100\Omega$$

9. Knee or cut in voltage

   Ge → 0.3 V

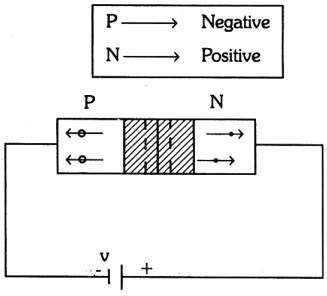
   Si → 0.7 V

10. Forward current equation

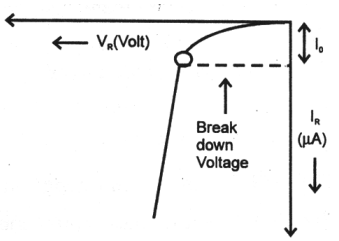
$$I = I_0\left[e^{+\frac{qv}{kt}} - 1\right] \quad e^{\frac{qv}{kt}} \gg 1$$

$$I \cong I_0 e^{\frac{qv}{kt}} \text{ (exp. increment)}$$

Reverse Bias



1. Potential Barrier increases.
2. Width of depletion layer increases.
3. P-N JN provide high resistance
4. Very small current flow.
5. Order of current micro amp.(Ge) or Nano amp.(Si)
6. Mainly minority current.
7. Reverse characteristic curve
8. Reverse resistance



$$R_B = \frac{\Delta V_B}{\Delta I_B} \cong 10^6\Omega$$

9. Breakdown voltage

   Ge → 25 V

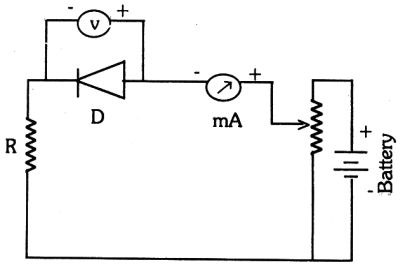
   Si → 35 V

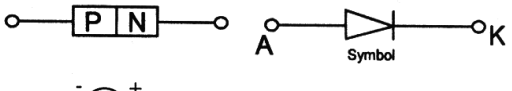
10. Reverse current equation

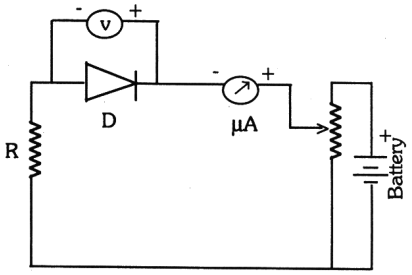
$$I = I_0\left[e^{-\frac{qv}{kt}} - 1\right]$$

$$e^{-\frac{qv}{KT}} << 1 \quad I \approx -I_0$$

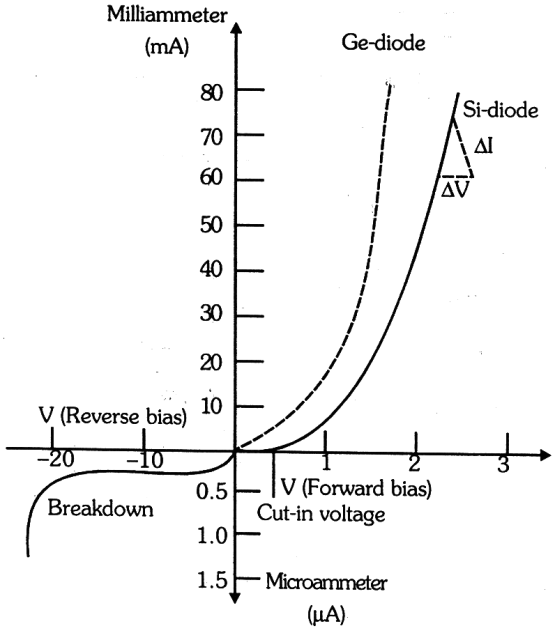
Characteristic curve of P-N junction diode :



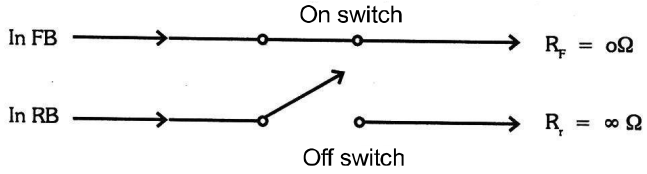




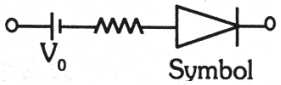
11.

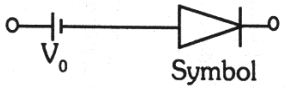


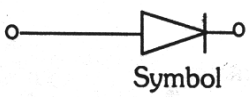
For ideal diode



MODEL

Approximate model 

Simplified model 

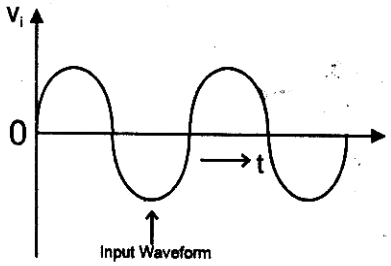
Ideal model 

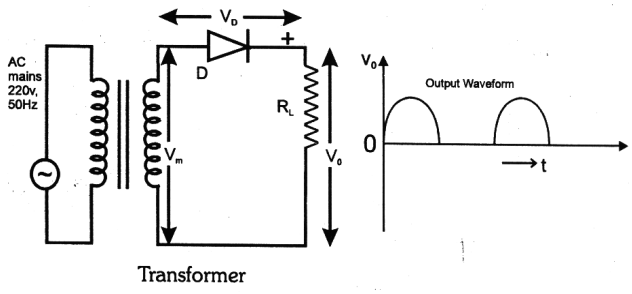
S.P. $\frac{R_R}{R_F} = 10^3 : 1$ for Ge $\frac{R_R}{R_F} = 10^4 : 1$ for Si

APPLICATION OF DIODE

1. RECTIFIER ⟶ Which converts AC into DC

(1) Half wave rectifier :





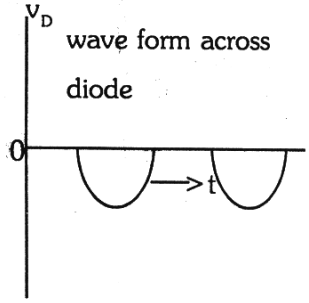
Transformer

(i) During positive half cycle

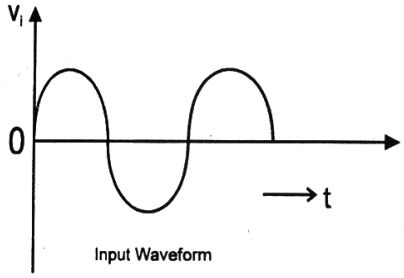
$D \rightarrow$ F.B. $\rightarrow$ On switch $\rightarrow$ output due to diode D

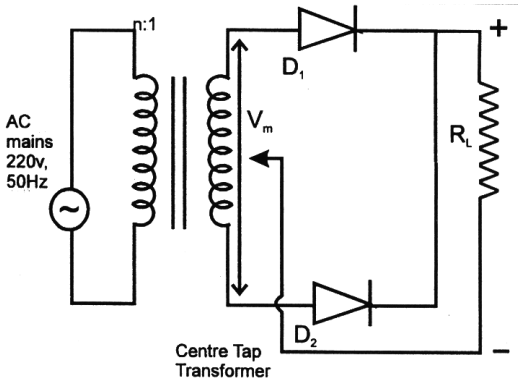
(ii) During Negative half cycle

$D \rightarrow$ R.B $\rightarrow$ off switch $\rightarrow$ No output



(2) Full wave rectifier :





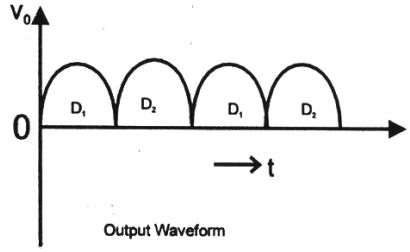
(i) During +ve half cycle

$D_1 \rightarrow$ F.B. $\rightarrow$ On switch
$D_2 \rightarrow$ R.B. $\rightarrow$ Off switch
] ouput due to diode D_1

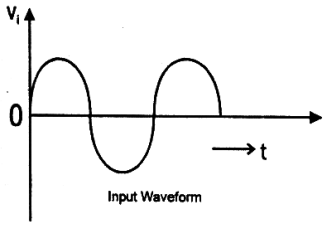
(i) During -ve half cycle

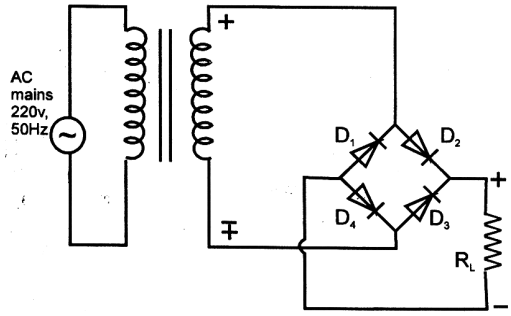
$D_1 \rightarrow$ R.B. $\rightarrow$ Off switch
$D_2 \rightarrow$ F.B. $\rightarrow$ On switch
] ouput due to diode D_2

$PIV = V_m = 2V_{in}$



(3) Bridge Rectifier :



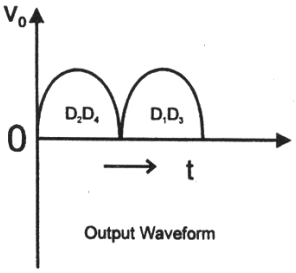


(i) During +ve half cycle

D_2 & $D_4 \rightarrow$ F.B. $\rightarrow$ on switch
D_1 & $D_3 \rightarrow$ R.B. $\rightarrow$ off switch
] ouput due to diode D_2 & D_4

(ii) During -ve half cycle

D_1 & $D_3 \rightarrow$ F.B. $\rightarrow$ on switch
D_2 & $D_4 \rightarrow$ R.B. $\rightarrow$ off switch
] ouput due to diode D_1 & D_3



2. RIPPLE & RIPPLE FACTOR :

In the output of rectifier some A.C. components are present. They are called ripple & there measurement is given by a factor so it is called ripple factor . for good rectifier ripple factor must be very low.

Total output current

$I_{rms} = \sqrt{I^2_{ac} + I^2_{dc}}$ I_{ac} = rms value of AC component

Ripple factor $f = \frac{I_{ac}}{I_{dc}}$ $r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

(i) For Half wave rectifier

$I_{rms} = \frac{I_0}{2}$, $I_{dc} = \frac{I_0}{\pi}$ $r = 1.21$

(ii) For full wave or bridge wave rectifier

$I_{rms} = \frac{I_0}{\sqrt{2}}$, $I_{dc} = \frac{2I_0}{\pi}$ $r = 0.48$

3 RECTIFIER EFFICIENCY

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I^2_{dc} R_L}{I^2_{rms}(R_F + R_L)}$$

Half wave rectifier	Full wave rectifier or bridge wave rectifier
$\eta = \frac{0.406}{1+\frac{R_f}{R_L}}$ if $\frac{R_f}{R_L} << 1$	$\eta = \frac{0.812}{1+\frac{R_f}{R_L}}$ if $\frac{R_f}{R_L} << 1$
$\eta = 40.6\%$	$\eta = 81.2\%$
special note If $R_f = R_L$	If $R_f = R_L$
$\eta = 20.3\%$	$\eta = 40.6\%$

Note; In bridge full wave rectifier R_f is two times of resistance of P-N Jn FB

4. FORM FACTOR

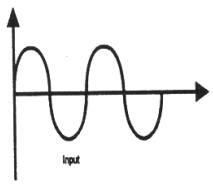
$F = \frac{I_{rms}}{I_{dc}}$ or $\frac{E_{rms}}{E_{dc}}$

$F = \frac{\pi}{2\sqrt{2}}$ for full wave rectifier

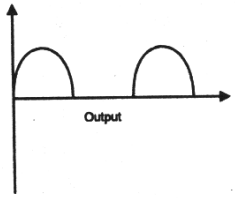
$F = \frac{\pi}{2}$ for half wave rectifier

5. RIPPLE FREQUENCY

(i) For half wave rectifier

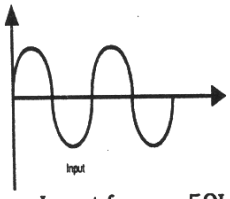


Input freq = 50Hz.

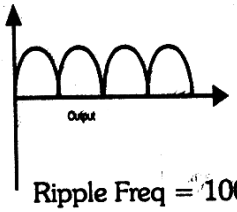


Ripple Freq = 50Hz.

(ii) For full wave rectifier



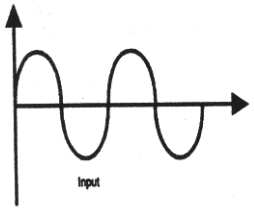
Input freq = 50Hz.



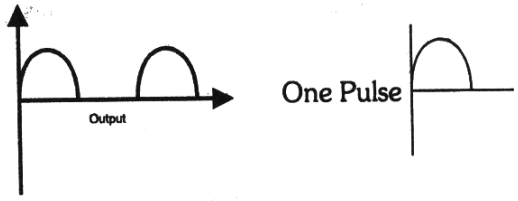
Ripple Freq = 100Hz.

6. Pulse : It is counting, no unit

(i) For half wave rectifier

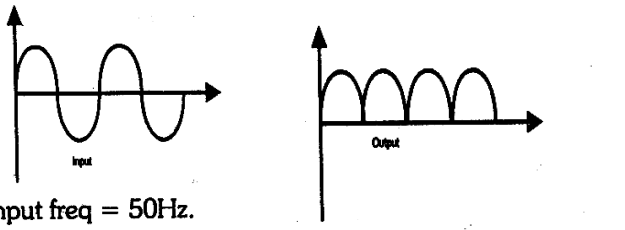


Input freq = 50Hz., No of Input Pulse = 100



No of Output pulses = 50

(ii) For full wave rectifier



Input freq = 50Hz.

No. of Input Pulses = 100

No of Output pulses = 100

Average current for H.W.R.

RMS current for H.W.R

$$\vec{I} = \frac{1}{T}\int_0^T I\,dt$$

$$\vec{I}^2 = \frac{1}{T}\int_0^T I^2 dt$$

$$\vec{I} = \frac{1}{T}\int_0^{T/2} I\,dt + \int_{T/2}^{T} I\,dt = \frac{1}{T}\int_0^{T/2} I_0 \sin\omega t\,dt + 0$$

$$= \frac{1}{T}\int_0^T \frac{2I_0^2 \sin^2 \omega t\,dt}{2}$$

$$= \frac{I_0}{T}\left[\frac{-\cos\omega t}{\omega}\right]_0^{T/2} = \frac{I_0}{\omega T}\left[-\cos\omega\frac{T}{2} + \cos 0\right]$$

$$= \frac{I_0^2}{2T}\left[\int_0^{T/2} (1-\cos 2\omega t)dt + 0\right]$$

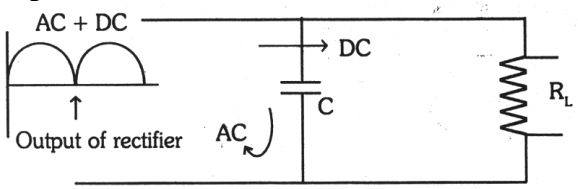
$$\vec{I} = \frac{I_0}{\pi} \qquad = \frac{I_0^2}{2T}\left[\frac{T}{2} - 0\right] \quad I_{rms} = \sqrt{\frac{I_0^2}{4}} = \frac{I_0}{2}$$

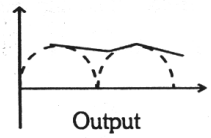
COMPARISON BETWEEN AVERAGE RECTIFIERS

		Full wave	
	Half - wave	**Centre- tap**	**Bridge**
Number of diodes	1	2	4
Transformer necessary	No	Yes	No
Peak secondary voltage	V_m	V_m	V_m
Peak load current, I_m	$V_{in}/(r_d+R_L)$	$V_{in}/(r_d+R_L)$	$V_{in}/(2r_d+R_L)$
RMS current, I_{rms}	$I_m/2$	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$
DC current, I_{dc}	I_m/π	$2I_m/\pi$	$2I_m/\pi$
Ripple factor, I_{dc}	1.21	0.482	0.482
Rectification efficiency (max)	40.6%	81.2%	81.2%
Lowest ripple frequency, f_r	f_i	$2f_i$	$2f_i$

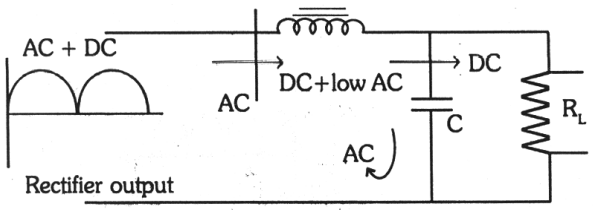
Filter circuit : To reduce AC components

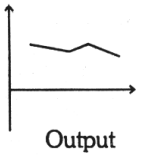
1. Capacitor Filter :



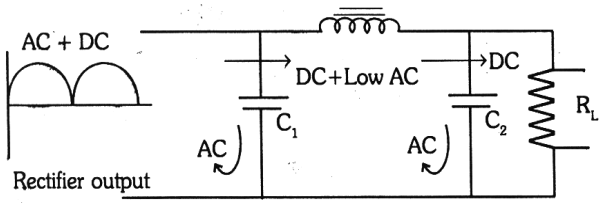


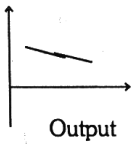
2. L- C Filter :





3. π - Filter (Best Filter)

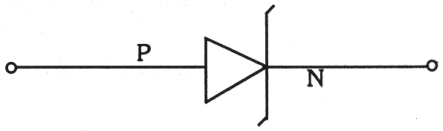




(Approx. pure D.C.)

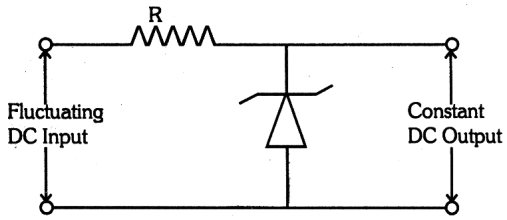
Zener Diode - C Zener

A properly doped crystel diode which has sharp Break down voltage is known as Zener diode.

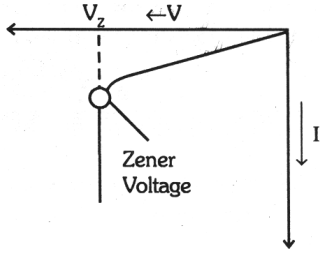


It is always connected R.B. manner.

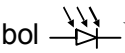
Used as a voltage regulation



In FB. it works as a simple diode.



SOME SPECIAL DIODES

* **Photodiode :** A junction diode made from "light or photo sensitive semiconductor" is called a "photo diode" its symbol  When light of energy "hν" falls on the photodiode (Here hν > energy gap) more electrons move from valence band, to conduction band, due to this current in circuit of photodiode in "Reverse bias", increases. As light intensity is increased, the current goes on increases so photo diode is used, "to detect light intensity" for example it is used in 'Video camera".

* **Light emitting diode (L.E.D) :** When a junction diode is "forward biased" energy is released at junction in the form of light due to recombination of electrons and holes. In case of Si or Ge diodes, the energy released is in infra-red region.

In the junction diode made of GaAs, InP etc energy is released in visible region such a junction diode is called "light emitting diode" (LED) Its symbol 

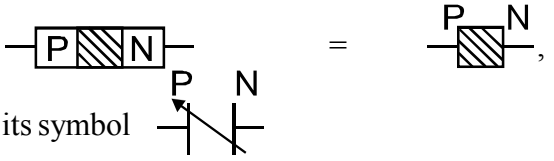
* **Solar cell :** Solar cell is a device for converting solar energy into electrical. A junction diode in which one of the P or N sections is made very thin (So that the light energy falling on diode is not greatly asorbed before reaching the junction) can be used to convert light energy into electric energy such diode called as solar cell. Its symbol 

(i) It is operated into photo voltaic mode i.e., generation of voltage due to the bombardment of optical photon.

(ii) No external bias is applied.

(iii) Active junction area is kept large, because we are interested in more power. Materials most commanly used for solar cell is Si, As, CdS, CdTe, CdSe, etc.

* **Variable capacitor (Variactor) :** P - N junction diode can be used as a "Capacitor" here depletion layer acts as "dielectric material" and remaining "P" and "N" part acts as metal plates.



Diode laser: - It is interesting form of LED in which' special construction helps to produce stimulated radiation as in laser.

Solved Examples

Ex.5 What will be conductance of pure silicon crystal at 300K Temp. If electron hole pairs per cm^3 is 1.072 × 10^{10} at this Temp; μ_n = 1350 cm^2/volt sec & μ_p = 480 cm^2 / volt sec

Sol. $\sigma = n_i e\mu_e + n_i e\mu_h$

$= n_i e(\mu_e + \mu_h) = 3.14 \times 10^{-6}$ mho/cm

Ex.6 A potential barrier of 0.5 V exists across a p-n junction (i) If the depletion region is 5 x 10^{-7} m wide. What is the intensity of the electric field in this region? (ii) An electron with speed 5 x 10^5 m/s approaches the p-n junction from the n-side with what speed will it enter the p-side.

Sol. (i) $E = \frac{V}{\Delta L} = \frac{0.5V}{5\times10^{-7}}$ Depletion layer = ΔL

$$E = 10^6 \ \frac{V}{m}$$

(ii) Work energy theorem

$$\frac{1}{2}MV_i^2 = eV + \frac{1}{2}MV_f^2$$

$$V_f = \sqrt{\frac{MV_i^2 - 2eV}{M}} \qquad = 2.7\times10^5 \text{ m/s}$$

Ex.7 Figure shows a diode connected to an external resistance and an e.m.f. Assuming that the barrier potential developed in diode is 0.5 V_1 obtain the value of current in the circuit in milliampere.

Sol. Here, E = 45 V_1 R = 100 Ω, voltage drop across p-n junction, = 0.5 V. Effective voltage in the circuit,

V = 4.5 – 0.5 = 4.0 V

current in the circuit,

$$I = \frac{V}{R} = \frac{4.0}{100} = 0.04A = 0.04 \times 1000 \text{ mA} = 40\text{mA}$$

TRANSISTOR

INTRODUCTION

I. **Transistor** is a three terminal device which is formed when a thin layer of one type of extrinsic semiconductor (P or N type is sandwitched between two thick layers of other two type extrinsic semiconductor. Each transistor have three terminals which are :

(i) Emitter (E) (ii) Base (B) (iii) Collector (C)

(i) **Emitter :-** It is the left most part of the transistor. It emit the majority carrier towards base. It is highly doped and medium in size.

(ii) **Base :-** It is the middle part of transistor which is sandwitched by emitter (E) and collector (C). It is lightly doped and very thin in size.

(iii) **Collector :-** It is right part of the transistor which collect the majority carrier which is emitted by emitter. It have large size and moderately doped.

There are two Semiconductor Junction :

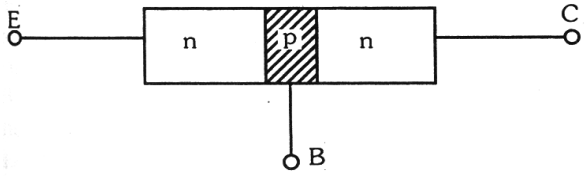
(i) The junction between emitter and base is known as emitter-base junction (J_{EB})

(ii) The junction between base & collector is known as base-collector junction (J_{CB})

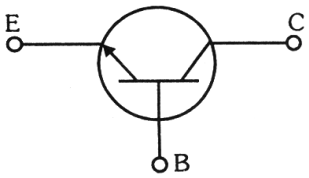
Types of transistor :- Transistor are two types

A. **N-P-N Transistor :**

If a thin layer of p-type semiconductor is sandwitched between two thick layer of n-type semiconductor is known as NPN transistor.

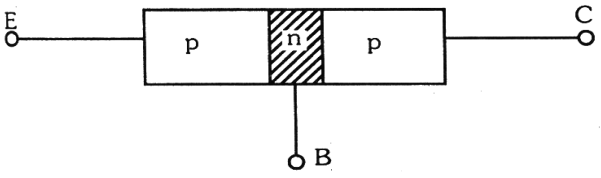


n-p-n Transistor

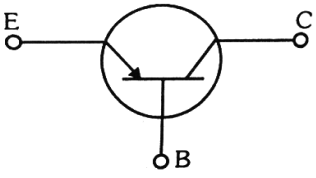


(Symbol)

B. **P-N-P Transistor :** If a thin layer of n-type of semiconductor is sandwitched between two thick layer of p-type semiconductor is known as PNP transistor.



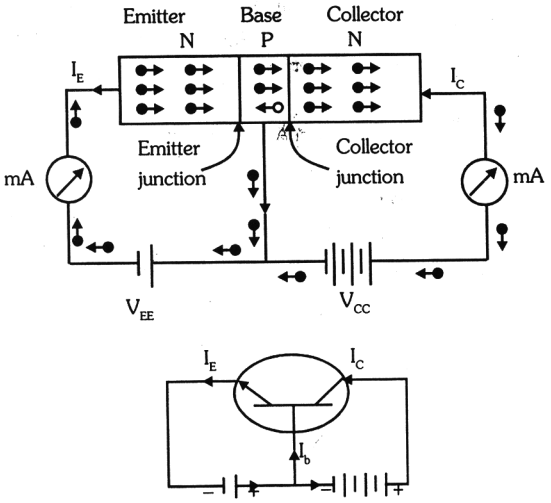
p-n-p Transistor



(Symbol)

1. WORKING OF TRANSISTOR :

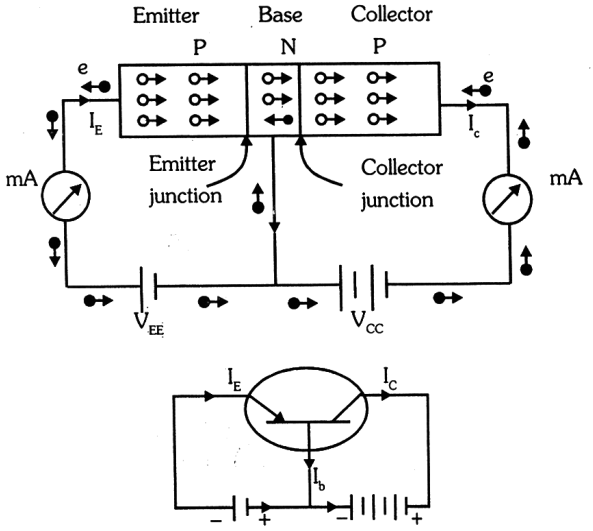
(a) Working of NPN Transistor :- The emitter Base junction is forward biased and collector base junction is reversed biased of n-p-n transistor in circuit (A) and symbolic representation is shown in Figure.



When emitter base junction is forward biased, electrons (majority carriers) in emitter are repelled towards base. The barrier of emitter base junction is reduced and the electron enter the base. About 5% of these electron recombine with hole in base region result in small current (I_b). The remaining electron ($\approx$ 95%) enter the collector region because they are attracted towards the positive terminal of battery. For each electron entering the positive terminal of the battery connected with collector base junction an electron from negative terminal, of the battery connected with emitter base junction enters the region. The emitter current (I_e) is more than the collector (I_c). The base current is the difference between I_e and I_c and proportional to the number of electron hole combination in the base.

$I_e = I_b + I_c$

(b) Working of PNP Transistor When emitter-base junction is forward biased holes (majority carriers) in the emitter are repelled towards the base and diffuse through the emitter base junction. The barrier potential of emitter-base junction decreases and hole enter the n-region (i.e. base). A small number of holes ($\approx$5%) combine with electron of n-region resulting small current (I_b). The remaining hole ($\approx$ 95%) enter into the collector region because they are attracted towards negative terminal of the battery connect with the collector-base junction. These holes constitute the collector current (I_c).



As one hole reaches the collector, it is neutralized by the battery. As soon as one electron and a hole neutralized in collector a covalent bond is broken in emitter region. The electron hole pair is produced. The released electron enter the positive terminal of battery and hole more towards the collector.

2. CHARACTERISTIC OF TRANSISTOR :

To study about the characteristic of transistor we have to make a circuit [i.e. $J_{EB} \rightarrow$ Forward bias and $J_{CB} \rightarrow$ Reverse bias] we need four terminal. But the transistor have three terminals. By keeping one of the terminal of transistor is common in input and output both. So the transistor is connected in three ways in circuit.

(i) Common Base connector (CB)

(ii) Common Emitter (CE)

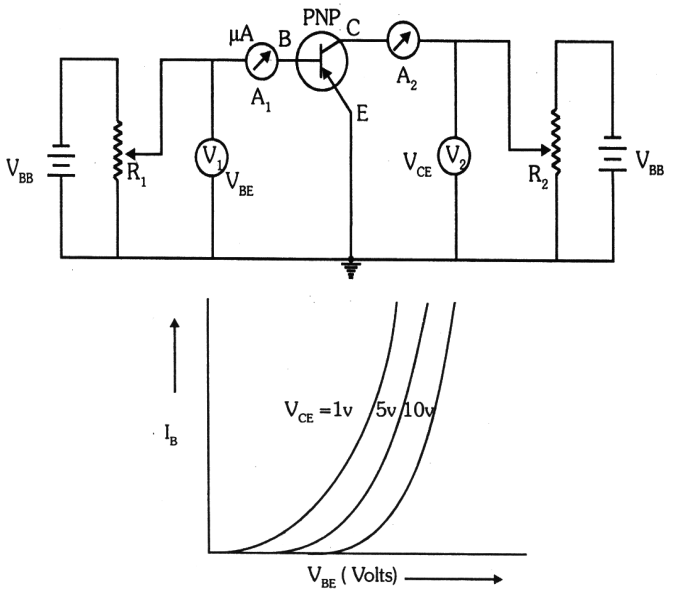
(iii)Common Collector (CC)

In these three CE is widely used and CC is rarely used.

Common Emitter characteristics of a transistor :

CE characteristic are two types:

1. **Input characteristics :-** The variation of base current (I_b) (input) with base emitter voltage (V_{EB}) at constant-emitter voltage (V_{CE}) is called input characteristics.



Input characteristic curve

(i) Keep the collector-emitter voltage (V_{CE}) constant (say V_{CE}) = 1 V)

(ii) Now change the emitter base voltage by R_1 and note the corresponding value of base current (I_b)

(iii) Plot the graph between V_{EB} and I_b.

(iv) A set of such curve can be plotted at different (V_{CE} = 2V)

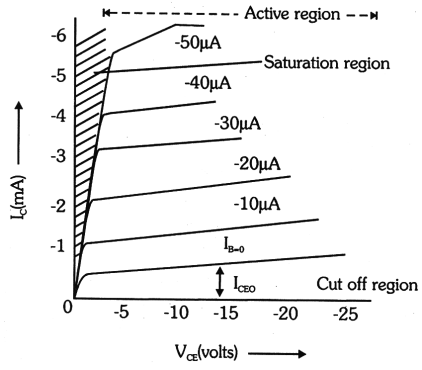
(2) Output characteristic :- The variation of collector current I_c (output) with collector-emitter voltage (V_{CE}) at constant base current (I_b) is called output characteristics.

(i) Keep the base current (I_b) constant (say I_b = 10μA)

(ii) Now change the collector-emitter voltage (V_{CE}) using variable resistance R_2 and note the corresponding values of collectors current (I_C).

(iii) Plot the graph between (V_{CE} v/s I_c)

(iv) A set of such curve can be plotted at different fixed values of base current (say 0, 20μA, 30μA etc.)



Important point :

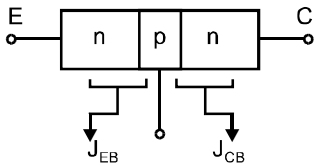
* Comparative study of E, B, C

Type of Terminal	Size	Doping
E	Medium	High
B	Smallest	Low
C	Largest	Medium

* The collector region is made physically larger than the emitter. Because collector has to dissipate much greater power.

* Transistor have two P-N Junction J_{EB} and J_{CB}. On the basis of junction condition transistor work in four region.

EB Jn.	CB Jn.	Region of working
(i) Forward Bias (FB)	Reverse Bias (RB)	Active
(ii) (FB)	(FB)	Inverse Active
(iii) (RB)	(RB)	Cut off
(iv) (FB)	(FB)	Saturation



* Transistors allmost work in active region in electronic devices & transistor works as an amplifier in Active region only.

* Transistor i.e. It is a short form of two words 'Transfer resistors". Signal is introduced at low resistance circuit and out put is taken at high resistance circuit.

* Base is lightly doped. Otherwise the most of the charge carrier from the emitter recombine in base region and not reaches at collector.

* Transistor is a current operated device i.e. the action of transistor is controlled by the motion of charge carriers. i.e. current (say 0, 20μA, 30μA etc.)

Input characteristic :

* In put characteristics is just similar to the forward characteristic of junction diode.
* For fixed value of V_{BE}, the base current I_b is decreases when we increase the V_{CE}'
* The ratio of change in V_{BE} to the small change in I_b is known as the, input resistance $(r_1) = \left(\frac{\Delta V_{BE}}{\Delta I_b}\right)$ it is inverse of slope of input characteristics.

Output characteristic :

* For given values of I_b, collector increase with V_{CE} in beginning but at high value of V_{CE} collector current becomes constant.
* Out put resistance $(r_0) = \left(\frac{\Delta V_{CE}}{\Delta I_c}\right)$

3. TRANSISTOR AS AN AMPLIFIER :

The process to increasing the amplitude of input signal without distorting its wave shape and without changing frequency is known as amplification. .

A device which increase the amplitude of the input signal is called.

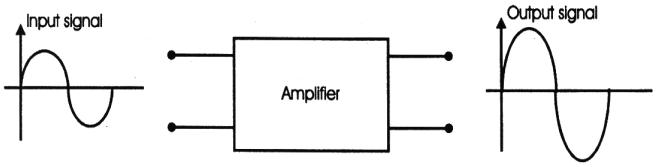
Amplifier are three:

(i) Common Emitter (CE) amplifier

(ii) Common Base (CB) amplifier

(iii) Common Collector (CC) amplifier

The device by which the amplitude of the signal at the output is mode greater than that if input signal is called amplifier.



Some of the important parameter of amplifier

1. Voltage gain (voltage amplification factor)

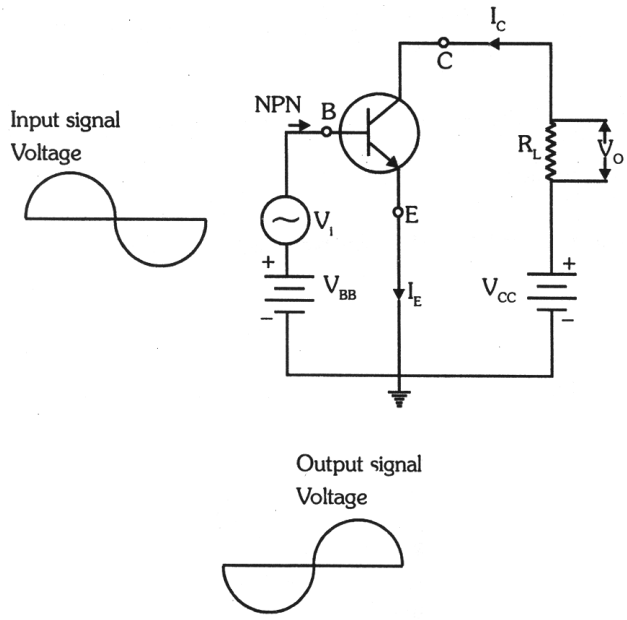
$$A_v = \frac{V_0}{V_{in}} = \frac{\text{Output voltage}}{\text{Input voltage}}$$

2. Current gain (current amplification factor)

3. Power gain (A_p)

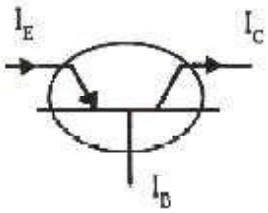
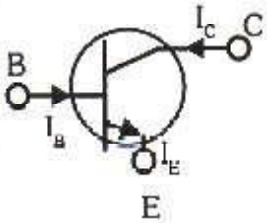
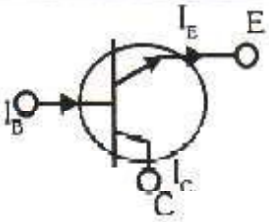
$$A_i = \frac{I_0}{I_{in}} \qquad A_p = \frac{\text{Output power}}{\text{Input power}}$$

C.E. AMPLIFIER :



Comparative study of transistor configuration

1. Common base (CB) 2. Common emitter (CE) 3.Common collector (CC)

			
1. Input Resistance	Low (100 Ω)	High (750 Ω)	Very High ≅ 750 KΩ
2. Output resistance	Very High	High	Low
3. Voltage Gain	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_B R_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_B R_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_E R_L}{I_B R_i}$
	$A_v = \alpha \frac{R_L}{R_i}$	$A_v = \beta \frac{R_L}{R_i}$	$A_v = \gamma \frac{R_L}{R_i}$
4. Current Gain	≅ 150 (A_i or α) $\alpha = I_C / I_b$ $\alpha < 1$	≅ 500 (A_i or β) $\beta = I_C / I_B$ $\beta > 1$	less than 1 (A_i or γ) $\gamma = I_b / I_B$ $\gamma > 1$
5. Power Gain	$A_p = \frac{P_o}{P_i}$	$A_p = \frac{P_o}{P_i}$	$A_p = \frac{P_o}{P_i}$
	$A_p = \alpha^2 \frac{R_L}{R_i}$	$A_p = \beta^2 \frac{R_L}{R_i}$	$A_p = \gamma^2 \frac{R_L}{R_i}$
6. Phase Diff. (O/P& I/P)	same phase	opp. phase	same phase
7. Application	For High Fequency	For Audioable fequency	for Impeadnance Matching

Relation Between α, β & γ

α , β	β , γ	α , γ
$I_E = I_B + I_C$	$I_E = I_B + I_C$	-
divide by I_C	divide by I_B	$\gamma = 1 + \frac{\alpha}{1-\alpha}$
$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$	$\frac{I_E}{I_B} = 1 + \frac{I_C}{I_B}$	$\boxed{\gamma = \frac{1}{1-\alpha}}$
$\frac{1}{\alpha} = \frac{1}{\beta} + 1$	$\boxed{\gamma = 1 + \beta}$	
$\boxed{\beta = \frac{\alpha}{1-\alpha}}$		

Important point:

* In transistor charge carriers moves from emitter to collector. Emitter send the charge carrier and collector collects them this happen only when emitter-base junction is forward bias and collector base junction is reverse bias (base of amplifier)
* In transistor reverse bias is high as compared to forward bias so that the charge carrier move from emitter to base exert a large attractive. force to enter in collector region so the base currant is very less.
* CE configuration is widely used because it have large voltage and power gain as compared to other amplifier.
* In amplifier negative feed back is used to stabilized the gain.
* $\gamma > \beta > \alpha$
* CC is used for impedance matching for connecting two transistor in caused.

Solved Examples

Ex.8 In a transistor, the value of β is 50. Calculate the value of α.

Sol. Here $\beta = 50$

Using $\beta = \frac{\alpha}{1-\alpha}$, we get

$50 = \frac{\alpha}{1-\alpha}$ or $50 - 50\,\alpha = \alpha$

or $51\alpha = 50 \quad \because \quad \alpha = \frac{50}{51} = 0.98$

Ex.9 Calculate the emitter current for which $I_b = 20\ \mu A$, $\beta = 100$

Sol. Here $\beta = 100$, $I_b = 20\ \mu A$

$\beta = \frac{I_c}{I_b} \quad \therefore I_c = \beta I_b = 100 \times 20 = 2000\ \mu A$

Using $I_e = I_b + I_c$, we get

$I_e = 20 + 2000 = 2020\ \mu A = 2.02 \times 10^{-3}$ A

$= 2.02$ mA

Ex.10 For a common emitter amplifier, current gain = 50. If the emitter current is 6.6 mA, calculate the collector and base current. Also calculate current gain, when emitter is working as common base amplifier.

Sol. Here, $\beta = 50$; $I_e = 6.6$ mA

Step-I since $\beta = \frac{I_c}{I_b}$

$\therefore I_c = \beta I_b = 50 I_b$ .....(1)

Step-II Now $I_e = I_c + I_b$

$\therefore 6.6 = 50\ I_b + I_b = 51 I_b$ (using equation 1)

or $I_b = \frac{6.6}{51} = 0.129$mA

Hence $I_c = 50 \times \frac{6.6}{51} = 6.47$mA

Stip-III $\beta = \frac{\alpha}{1-\alpha}$ or $\alpha = \frac{\beta}{1+\beta} = \frac{50}{51} = 0.98$

Ex.11 Transistor with $\beta = 75$ is connected to common-base configuration. What will be the maximum collector current for an emitter current of 5mA ?

Sol. Here $\beta = 75$, $I_e = 5$mA

Step-I Using $\beta = \frac{\alpha}{1-\alpha}$, we get

$75 = \frac{\alpha}{1-\alpha}$ or $75 - 75\,\alpha = \alpha$

or $75\,\alpha = 75$

or $\alpha = \frac{75}{76}$

Step-II $\alpha = \frac{I_c}{I_e} \quad \therefore$

$I_c = \alpha I_e = \frac{75}{76} \times 5 = 4.93$ A

Ex.12 The base current is 100 μA and collector current is 3mA.

(a) Calculate the values of β, I_e and α

(b) A change of 20 μA in the base current produces a change of 0.5 mA is the collector current. Calculate $\beta_{ac.}$

Sol. Here $I_b = 100\mu A = 0.100$ mA

$I_c = 3$mA

(a) Using $\beta = \frac{I_c}{I_b}$, we get $\beta = \frac{3}{0.100} = 30$

Using $\beta = \frac{\alpha}{1-\alpha}$, wet get

$$30 = \frac{\alpha}{1-\alpha} = 30 - 30\alpha = \alpha$$

or $31\alpha = 30 \quad \therefore \ \alpha = \frac{30}{31} = 0.97$

Using $\alpha = \frac{I_c}{I_e}$, we get

$$I_e = \frac{I_c}{\alpha} = \frac{3 \times 31}{30} = 3.1\,mA$$

(b) Here $\Delta I_b = 20\mu A = 0.02mA$

$\Delta I_c = 0.50mA$

$$\therefore \ \beta_{ac} = \frac{\Delta I_c}{\Delta I_b} = \frac{0.5}{0.02} = 25$$

Ex.13 In npn transistor circuit, the collector current is 10 mA. If 95% of the electrons emitted reach the collector, what is the base current ?

Sol. Setp-I $I_c = 65\% \quad I_e = 0.95 I_e$

$\therefore \ I_e = \frac{I_c}{0.95} = \frac{10}{0.95}$ ($\because I_c = 10mA$) =10.53mA

Setp-II Now $I_e = I_c + I_b$

$\therefore \ I_b = I_e - I_c \quad = 10.53 - 10 = 0.53mA$

Ex.14 In an NPN transistor 10^{10} electrons enter the emitter in 10^{-6} s and 2% electrons recombine with holes in base, then current gain α and β are :

Sol. Emitter current $I_E = \frac{Ne}{t} \quad \frac{10^{10} \times 1.6 \times 10^{-19}}{10^{-6}}$

= 1.6mA

Base current $I_B = \frac{2}{100} \times 1.6mA = 0.032$ mA

but$I_E = I_C + I_B$

$\therefore \ I_C = I_E - I_B = 1.6 - 0.032 = 1.568$ mA

$$\therefore \ \alpha = \frac{I_C}{I_E} = \frac{1.568}{1.6} = 0.98 \quad \therefore \beta = \frac{I_C}{I_B} = \frac{1.568}{0.032} = 49$$

Feedback :- Feedback is of two type :

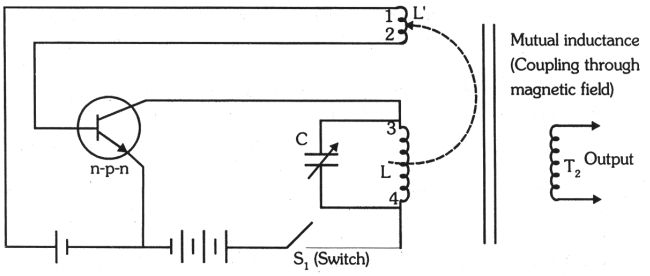
i. **Positive feedback :-** When input and output are in the same phase then positive feedback is there. It is used in oscillators.

ii. **Negative feedback :-** If input and output are out of phase and some part of that is fedback to input is known as negative feedback. It is used to get constant gain amplifier.

4. TRANSISTOR IN AN OSCILLATOR CIRCUIT :

Oscillator is device which delivers a.c. output wave form of desired frequency from d.c. power even without input signal excitation.

The electric oscillations are produced by L-C circuit (i.e. tank circuit containing inductor and capacitor). These oscillations are damped one i.e. their amplitude decrease with the passage of time due to the small resistance of the inductor. In other words, the energy of the L-C oscillations decreases. If this loss of energy is compensated from outside, then undamped oscillations decreases. If this loss of energy is compensated from outside, then undamped oscillations (of constant amplitude) can be obtained. This can be done by using feed back arrangement and a transistor in the circuit.



L-C circuit producing L-C oscillations consists of an inductor of inductance L and capacitor of variable capacitance.Inductor of inductance L' is connected in the collector-emitter circuit through a battery and a tapping key (K). Inductors L and L' are inductively coupled (Figure)

Working :- When key K is closed, collector current begins to flow through the coil L'. As this current grows, magnetic flux linked with coil L' increase (i.e. changes). Since coil 1 is inductively coupled with L', so magnetic flux linked with coil L also changes. Due to change in magnetic flux, induced e.m.f. is set up across the coil L. The direction of induced e.m.f. is such that the emitter-base junction is forward biased. As a result of this biasing, emitter current I_e increases which in turn increases the collector current I_c [$\because I_e = I_b + I_c$]

With the increase in collector current, magnetic flux linked with coil L' also increases. This increases the e.m.f. induced in the coil L. The increased induced e.m.f. increases the forward bias of emitter base junction. Hence emitter current is further increased which in turn increases the collector current. The process of increasing the collector current continues till the magnetic flux linked with coil L' becomes maximum (i.e. constant). At this stage, the induced e.m.f. in coil L becomes zero. The upper plate of the capacitor C gets positively charged during this process. When induced e.m.f. becomes zero, the capacitor C starts discharging through the inductor L. The. emitter current starts decreasing resulting in the collector current. With decreasing collector current which flows through L', e.m.f. is again induced produced in the coil L but in the opposite direction. It opposes the emitter current and hence collector current ultimately decreases to zero. The change in magnetic flux linked with coil L' stops and hence induced e.m.f. in the coil L becomes zero. At this stage, the capacitor gets discharged through coil L but now in the opposite direction. Now the emitter current and hence collector current increase but now in the opposite direction .This process repeats and the collector current oscillates between maximum and minimum values.

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Advantages and disadvantages of Semiconductor devices over Vacuum tubes :

Advantage:

* Semiconductor devices are very small in size as compared to the vacuum tubes. Hence the circuits using semiconductor devices are more compact.
* In vacuum tubes, current flows when the filament is heated and starts emitting electrons. So, we have to wait for some time for the operation of the circuit. On the other hand, in semiconductor devices no heating is required and the circuit begins to operate as soon as it is switched on.
* Semiconductor devices require low voltage for their operation as compared to the vacuum tube. So lot of electrical power is saved.
* Semiconductor devices do not produce any humming noise which is large in case of vacuum tube.
* Semiconductor devices have longer life than the vacuum tube. Vacuum tube gets damaged when its filament is burnt.
* Semiconductor devices are shock proof.
* The cost of production of semiconductor-devices is very small as compared to the vacuum tubes.
* Semiconductor devices can be easily transported as compared to vacuum tube.

Disadvantage:

* Semiconductor devices are heat sensitive. They get damaged due to overheating and high voltages. So they have to be housed in a controlled temperature room.
* The noise level in semiconductor devices is very high.
* Semiconductor devices have poor response in high frequency range.

LOGIC GATE

INTRODUCTION

A logic gate is a digital circuit which is based on certain logical relationship between the input and the output voltages of the circuit.

The logic gates are built using the semiconductor diodes and transistors.

Each logic gate is represented by tits characteristic symbol.

The operation of a logic gate is indicated in a table, known as truth table. This table contains all possible combinations of inputs and the corresponding outputs.

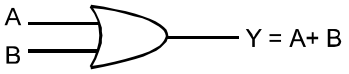
A logic gate is also represented by a Boolean algebraic expression. Boolean algebra is a method of writing equations showing how an output depends upon the combination of inputs. Boolean algebra was invented by George Boole.

Basic logic gates

(1) OR gate (2) AND gate, and (3) NOT gate

The OR gate : - The output and an OR gate attains the state 1 if one or more inputs attain the state 1.

Logic symbol of OR gate



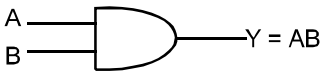
The Boolean expression of OR gate is Y = A + B, read as Y equals A or B.

Truth table of a two input OR gate

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

The AND gate : The output of an AND gat attains the state 1 if and only if all the inputs are in state 1.

Logic symbol of AND gate



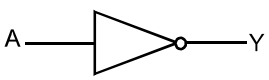
The Boolean expression of AND gate is Y = A.B It is read as Y equal A and B

Truth table of a two input AND gate

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

The NOT gate : The output of a NOT gate attains the state 1 if and only if the input does not attain the state 1.

Logic symbol of NOT gate



The Boolean expression is $Y = \overline{A}$, read as Y equals NOT A.

Truth table of NOT gate

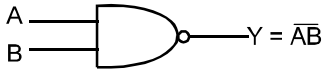
Input	Output
A	B
0	1
1	0

COMBINATION OF GATES :

The three basis gates (OR, AND and NOT) when connected in various combinations give us logic gates such as NAND, NOR gates, which are the universal building blocks of digital circuits.

The NAND gate

Logic symbol of NAND gate



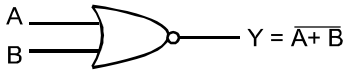
The Boolean expression of NAND gate is $Y = \overline{AB}$

Truth table of a NAND gate

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

The NOR gate :

Logic symbol of NOR gate



The Boolean expression of NOR gate is $Y = \overline{A+B}$

Truth table of a NOR gate

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

UNIVERSAL GATES :

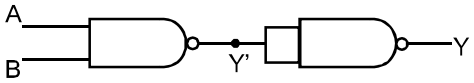
The NAND or NOR gate is the universal building block of all digital circuits. Repeated use of NAND gates (or NOR gates) gives other gates. Therefore, any digital system can be achieved entirely from NAND or NOR gates. We shall show how the repeated use of NAND (and NOR) gates will gives use different gates.

The NOT gate from a NAND gate : When all the inputs of a NAND gate are connected together, as shown in the figure, we obtain a NOT gate

Truth table of single-input NAND gate

Input		Output
A	B = (A)	Y
0	0	1
1	1	0

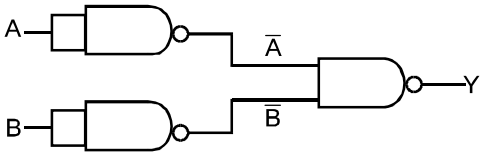
The AND gate from a NAND gate : If a NAND gate is followed by a NOT gate (i.e., a single input NAND gate), the resulting circuit is an AND gate as shown in figure and truth the table given show how an AND gate has been obtained from NAND gates.



Truth table

A	B	Y'	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

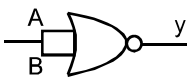
The OR gate from NAND gate : If we invert the inputs A and B and then apply them to the NAND gate, the resulting circuit is an OR gate.



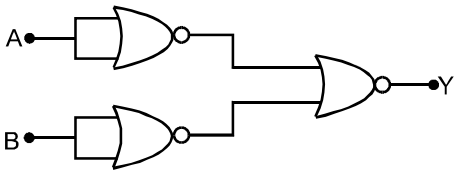
Truth table

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

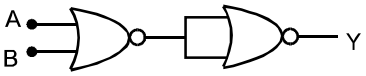
The NOT gate from NOR gates : When all the inputs of a NOR gate are connected together as shown in the figure, we obtain a NOR gate.



The AND gate from NOR gates : If we invert the inputs A and B and then apply them to the NOR gate, the resulting circuit is an AND gate.



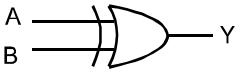
The OR gate from NOR gate : If a NOR gate is followed by a single input NOR gate (NOT gate), the resulting circuit is an OR gate.



XOR AND XNOR GATE :

The exclusive - OR gate (XOR gate) : The output of a two -input XOR gate attains the state 1 if one and only one input attains the state 1.

Logic symbol of XOR gate



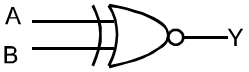
The Boolean expression of XOR gate is $Y = A\overline{B} + \overline{A}B$ or $Y = A \oplus B$

Truth table of a XOR gate

Input		Ouput
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive : NOR gate (XNOR gate) The output is in state 1 when its both input are the same that is, both 0 or both 1.

Logic symbol of XNOR gate



The Boolean expression of XNOR gate is Y = A.B + $\overline{A}.\overline{B}$ or Y = $\overline{A \oplus B}$

Truth table of a XNOR gate

Input		Ouput
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Laws of Boolean Algebra

Basic OR, AND, and NOT operations are given below :

OR	AND	NOT
$A + 0 = A$	$A.\ 0 = 0$	$A + \bar{A} = 1$
$A + 1 = 1$	$A.\ 1 = 1$	$A.\ \bar{A} = 0$
$A + A = A$	$A\ .\ A = A$	$\bar{\bar{A}}\ .\ A = A$

Boolean algebra obeys commutative, associative and distributive laws as given below :

Commutative laws :

$A + B = B + A$;

$AB = BA$

Associative laws :

$A + (B + C) = (A + B) + C$;

$A.\ (B.\ C) = (A.\ B).\ C$

Distributive laws :

$A\ (B + C) = AB + AC$

Some other useful identities :

(i) $A + AB = A$;

(ii) $A.\ (A + B) = A.$

(iii) $A + \bar{A}B = A + B$

(iv) $A.\ (\bar{A} + B) = AB$

(v) $A + BC = (A + B)\ (A + C)$

(vi) $(\bar{A} + B)\ (A + C) = \bar{A}C$

De Morgan's theorem :

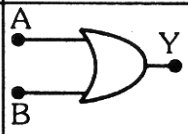
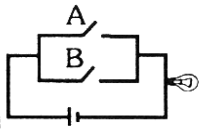
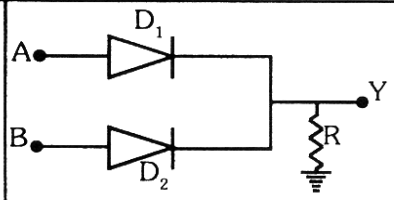
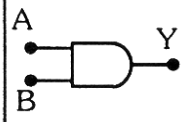
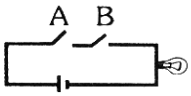
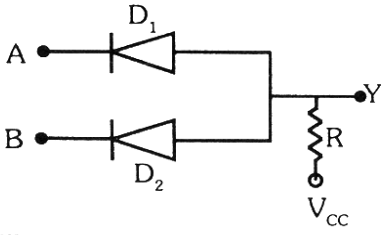
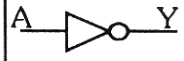
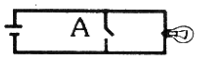
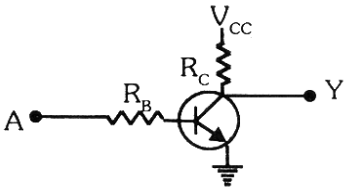
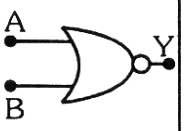
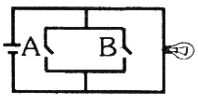
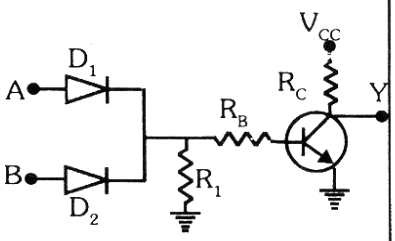
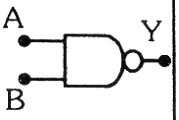
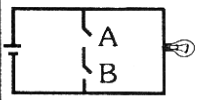
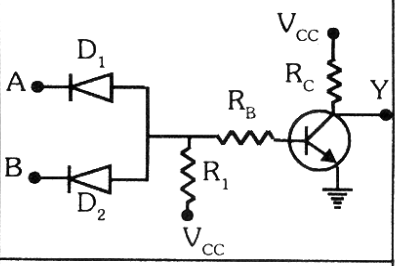
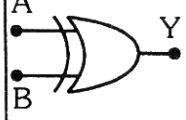
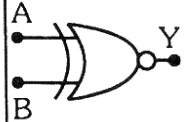
First theorem :

$\overline{A+B} = \overline{A}.\overline{B}$

Second theorem :

$\overline{A.B} = \bar{A} + \bar{B}$

RAPID REVISION PACKAGE

Names	Symbol	Boolean Expression	Truth table	Electrical analogue	Circuit diagram (Practical Realisation)
OR		$Y = A + B$	A B Y 0 0 0 0 1 1 1 0 1 1 1 1		
AND		$Y = A.B$	A B Y 0 0 0 0 1 0 1 0 0 1 1 1		
NOT or Inverter		$Y = \overline{A}$	A Y 0 1 1 0		
NOR (OR +NOT)		$Y = \overline{A + B}$	A B Y 0 0 1 0 1 0 1 0 0 1 1 0		
NAND (AND+NOT)		$Y = \overline{A.B}$	A B Y 0 0 1 0 1 1 1 0 1 1 1 0		
XOR (Exclusive OR)		$Y = A \oplus B$ or $Y = \overline{A}.B + A\overline{B}$	A B Y 0 0 0 0 1 1 1 0 1 1 1 0		
XNOR (Exclusive NOR)		$Y = \overline{A \oplus B}$ or $Y = A.B + \overline{A}.\overline{B}$	A B Y 0 0 1 0 1 0 1 0 0 1 1 1		