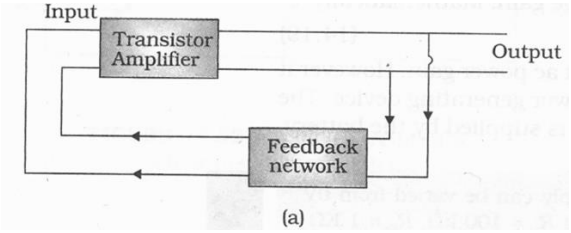
SEMICONDUCTOR ELECTRONICS

AMPLIFIER & LOGIC GATE

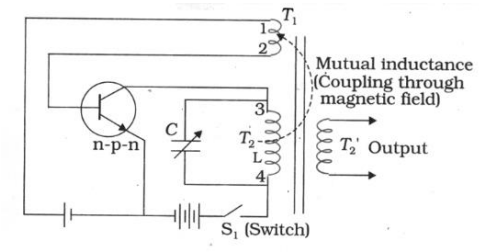
FEEDBACK AMPLIFIER AND TRANSISTOR OSCILLATOR:

Within an oscillator, an alternating current (AC) output is generated in the absence of external input signals. This distinctive functionality arises from a mechanism wherein a fraction of the output power is redirected back to the input, aligning in phase with the initial power. This specific procedure is denoted as positive feedback, and its representation is illustrated in figure (a). The establishment of feedback can be accomplished through various means such as inductive coupling, which involves mutual inductance, or through the utilization of LC (inductance-capacitance) or RC (resistance-capacitance) networks. These feedback methods contribute to the self-sustaining nature of the oscillator, enabling the continuous generation of AC output without the need for external stimuli.



(a)

Let's consider the scenario where switch S1 is engaged to apply the necessary bias for the initial activation. Understandably, as a result of this action, a surge of collector current is initiated within the transistor. This particular current path directs itself through the coil denoted as T2, with terminals labeled as 3 and 4 in Figure b. The flow of current through this coil is a consequential part of the activation process triggered by the engagement of switch S1, contributing to the dynamic behavior of the system.

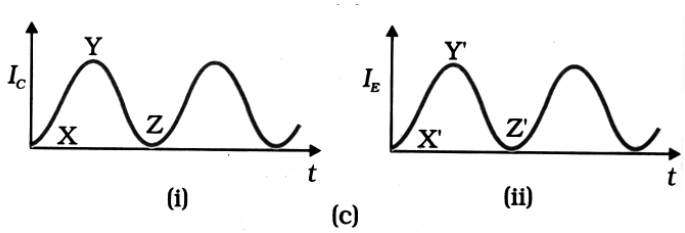


(b)

The surge of collector current initiated by the engagement of switch S1 doesn't reach its maximum amplitude immediately. Instead, it gradually escalates from point X to point Y, as depicted in Figure (C). During this progression, the inductive coupling between coil T2 and coil T1 comes into play, leading to the generation of a current within the emitter circuit. It's crucial to note that this emerging current in the emitter circuit constitutes the 'feedback' mechanism, forming a connection from the input to the output.

As a consequence of this positive feedback mechanism, the current in the emitter circuit (referred to as T1 emitter current) also undergoes an incremental increase from point X' to point Y', as illustrated in Figure (C) (ii).

This intricate interplay of currents and feedback mechanisms contributes to the dynamic evolution of the system, showcasing the complexity inherent in the operation of the circuit.



When the transistor T_2 reaches saturation, the current flowing through its collector circuit attains the value Y, signifying that the maximum collector current is achieved and can no longer increase. At this point, the magnetic field surrounding T_2 ceases to expand, as the collector current remains constant. Consequently, the feedback loop from T_2 to T_1 be interrupted because the static magnetic field no longer induces further feedback.

As the feedback diminishes, the emitter current begins to decline. This reduction in emitter current results in a decrease in collector current, causing the magnetic field around coil T_2 to decay. Now, T_1 perceives a diminishing field in T_2, which is contrary to the initial operation when the field was growing. This leads to a simultaneous decline in both emitter current (IE) and collector current (IC), causing the transistor to revert to its original state as it was when the power was initially switched on.

This entire sequence of events repeats cyclically. The transistor undergoes a process of being driven to saturation, transitioning to cut-off, and then returning to saturation. The duration of the transition from saturation to cut-off and back is determined by the time constant of the tank circuit or tuned circuit, represented by the inductance (L) of Coil T_2 and the capacitance (C) connected in parallel to it. The resonance frequency (ν) of this tuned circuit governs the frequency at which the oscillator oscillates and can be expressed as $\nu = \frac{1}{2\pi\sqrt{LC}}$

Logic Gates:

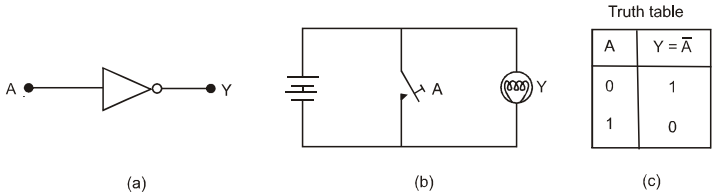
A logic gate is a digital circuit which works according to some logical relationship between Input and output voltages. It either allows a signal to pass through or stops it. A gate is a Digital circuit that follows curtain logical relationship between the input and output Voltages. Therefore, they are generally known as logic gates — gates because they control the flow of information. The five common logic gates used are NOT, AND, OR, NAND, NOR. Each logic gate is indicated by a symbol and its function is defined by a truth table that shows all the possible input logic level combinations with their respective output logic levels. Truth tables help understand the behavior of logic gates. These logic gates can be realised using semiconductor devices.

(a) The NOT Gate:

The NOT gate is a fundamental logical component featuring a solitary input (A) and a single output (Y). It operates in accordance with the Boolean expression "NOT A equals Y," indicating that the output Y is the negation or inversion of the input A.

In practical terms, when A is 1, the output Y becomes 0, and when A is 0, the output Y becomes 1. This binary relationship arises due to the limited binary system consisting of only two digits, 0 and 1.

In essence, the NOT gate functions to complement the input signal. If the input is in a true state (1), the NOT gate transforms it into a false state (0), and vice versa. This behavior is crucial in digital logic operations, where logical states are manipulated to perform various computational tasks. The logic symbol representing the NOT gate is depicted in the accompanying figure.



The various combinations of input A and the resulting output Y for the NOT gate can be elucidated through the implementation of an electric circuit, illustrated in the provided figure. This circuit comprises a switch (representing input A) connected in parallel to both a battery and a bulb (representing output Y). The operational dynamics of the circuit can be delineated as follows:

1. When the switch A is in an open position ($A = 0$), electric current flows through the circuit, causing the bulb to illuminate ($Y = 1$).

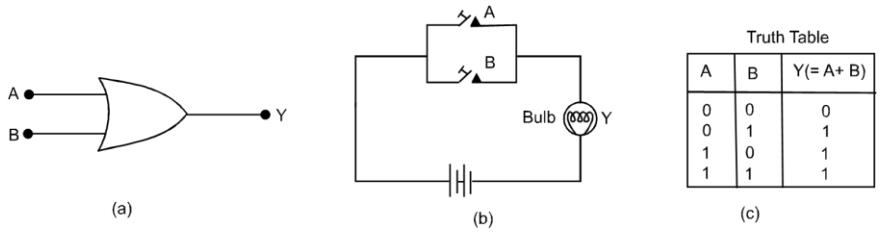
2. Conversely, when the switch A is closed ($A = 1$), the circuit is interrupted, preventing the flow of electric current and resulting in the bulb not emitting light ($Y = 0$).

These two distinctive scenarios of input A and corresponding output Y are systematically organized in a tabulated form, presented in the accompanying figure. This tabulation effectively encapsulates the truth table of the NOT gate, outlining the logical relationships between input and output states in a comprehensible manner.

(b) The OR Gate:

The OR gate is a logical component characterized by two input variables, denoted as A and B, and a single output variable, represented as Y. Its operational logic adheres to the Boolean expression $A + B = Y$, which is interpreted as 'A OR B equals Y'. This expression signifies that the output Y is the result of the logical OR operation applied to inputs A and B.

In practical terms, the output Y of the OR gate assumes a true (1) state if either input A or input B, or both, are in a true state. Conversely, if both inputs A and B are in a false state (0), the output Y remains in a false state. The logic symbol representing the OR gate is visually depicted in the accompanying figure. This symbol serves as a concise representation of the gate's logical function, facilitating its incorporation into digital circuit diagrams and logical operations.



The potential permutations of input combinations A and B, along with the resultant output Y of the OR gate, can be discerned through the implementation of an electrical circuit, as illustrated in the provided figure. This circuit features two switches, denoted as A and B (representing the inputs), which are connected in parallel to both a battery and a bulb Y (indicating the output).

The functionality of the circuit can be elucidated as follows:

1. If either switch A or switch B, or both, are in the closed position, thereby completing the circuit ($A = 1$ or $B = 1$), electric current flows, causing the bulb to illuminate ($Y = 1$).

2. Conversely, if both switches A and B are in the open position, breaking the circuit ($A = 0$ and $B = 0$), the flow of electric current is interrupted, resulting in the bulb not emitting light ($Y = 0$).

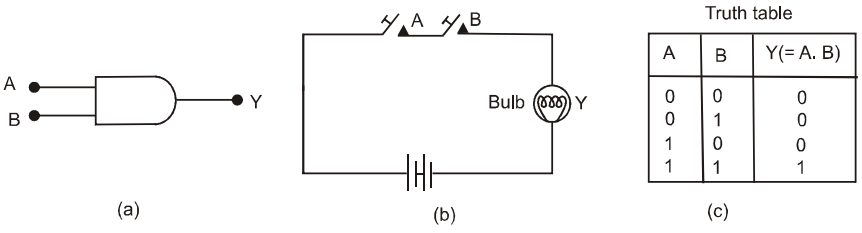
This circuit configuration effectively demonstrates the logical OR operation, wherein the output Y assumes a true state if at least one of the inputs A or B is in a true state. The visual representation of this circuit aids in understanding the diverse input-output scenarios of the OR gate, providing valuable insights into its logical behavior.

(c) The AND Gate:

The AND gate, like the OR gate, is a logical component with two inputs, A and B, and a single output, denoted as Y. Its operational logic adheres to the Boolean expression $A.B = Y$, which can be read as 'A AND B equals Y.' This Boolean expression signifies that the output Y is the result of the logical AND operation applied to inputs A and B.

In practical terms, the output Y of the AND gate assumes a true (1) state only when both inputs A and B are in a true state. If either input A or input B, or both, are in a false state (0), the output Y remains in a false state. The logic symbol representing the AND gate visually portrays its logical function and is an integral part of digital circuit diagrams.

This gate plays a crucial role in logical operations, where the combination of true and false states in the inputs yields specific outcomes based on the logical AND relationship between the inputs.



Combinations of gates:

Diverse arrangements of the three fundamental logic gates, namely OR, AND, and NOT, give rise to intricate digital circuits often referred to as 'gates.' Combinations of these basic gates are frequently utilized in the construction of more complex logic circuits. Notably, the NAND gate and the NOR gate are commonly employed configurations and are recognized as universal gates.

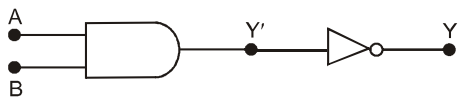
The NAND gate is formed by combining an AND gate followed by a NOT gate, resulting in an output that is the inversion of the logical AND operation between its inputs. On the other hand, the NOR gate is created by combining an OR gate followed by a NOT gate, yielding an output that is the negation of the logical OR operation between its inputs.

These NAND and NOR gates are deemed universal because any logical function can be implemented using them alone. In essence, they provide a versatile foundation for constructing a wide array of digital circuits, showcasing their significance in the realm of digital logic design.

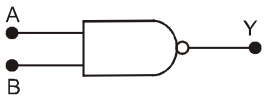
(i) The NAND gate:

The NAND gate is a composite construct involving the combination of an AND gate followed by a NOT gate. In the configuration of a NAND gate, the output Y' (complement of Y) from the AND gate is directly linked to the input of a NOT gate, as depicted in the accompanying figure. This linkage results in a logical operation where the output of the NAND gate is the negation of the logical AND operation performed on its inputs.

Visually, the logic symbol representing the NAND gate is illustrated in the figure, serving as a succinct representation of its logical function. This symbol is instrumental in the representation and interpretation of digital circuit diagrams, where the NAND gate finds widespread use due to its ability to perform various logical operations and its versatility in constructing complex digital circuits.



(a)



(b)

The Boolean expression that characterizes the NAND gate is expressed as 'A AND B negated equals Y.' this expression conveys that the output Y of the NAND gate is derived from the negation of the logical AND operation applied to its input variables A and B.

To construct the truth table for the NAND gate, one can systematically combine the truth tables of the constituent AND NOT gates. In the provided figure, the output Y' from the truth table of the AND gate undergoes a negation operation (NOT) to produce the corresponding outputs Y for the NAND gate. The resultant table, which outlines the relationship between input combinations (A and B) and the resulting output Y for the NAND gate, is thereby established.

This truth table serves as a comprehensive reference, detailing the logical outcomes associated with various input scenarios for the NAND gate. It encapsulates the essence of the NAND gate's behavior and aids in understanding its role within digital circuits.

A	B	Y′ (= A. B)	Y (= $\overline{A.B}$) = $\overline{Y'}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

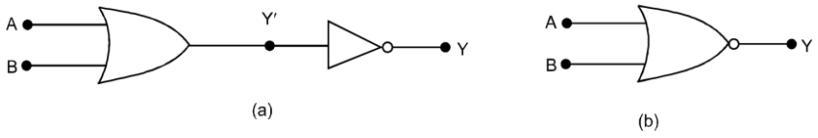
⇒

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(ii) The NOR Gate:

The NOR gate is a composite logical construct formed by integrating an OR gate with a NOT gate. In the configuration of a NOR gate, the output Y' (complement of Y) from the OR gate is directly linked to the input of a NOT gate, as depicted in the provided figure. This arrangement results in a logical operation where the output of the NOR gate is the negation of the logical OR operation applied to its input variables.

Visually, the logic symbol representing the NOR gate is illustrated in the figure, serving as a concise representation of its logical function. This symbol is instrumental in the representation and interpretation of digital circuit diagrams, where the NOR gate finds widespread application due to its ability to perform various logical operations and its versatility in constructing complex digital circuits.



The Boolean expression defining the NOR gate is expressed as 'A OR B negated equals Y.' this expression signifies that the output Y of the NOR gate results from the negation of the logical OR operation applied to its input variables A and B. In simpler terms, the NOR gate produces a true output (1) only when both input variables A and B are false (0), and it generates a false output (0) when at least one of the inputs is true. This Boolean expression encapsulates the fundamental logic governing the NOR gate's behavior, emphasizing its role in digital circuitry where it serves to perform specific logical operations.

A	B	Y′ (= A+B)	Y (= $\overline{A+B}$) = $\overline{Y'}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

The truth table for the NOR gate is derived through the logical combination of the truth tables associated with the OR and NOT gates. In Figure (a), the outputs Y' from the truth table of the OR gate are subjected to a negation operation (NOT) to yield the corresponding outputs Y for the NOR gate.

To elaborate, the truth table of the OR gate outlines the logical outcomes for various combinations of input variables A and B, while the negation operation on the OR gate's outputs generates the complementary values for these outcomes, forming the truth table for the NOR gate.

This resulting truth table provides a comprehensive representation of the NOR gate's behavior, delineating the relationship between input combinations and the resulting output states. It is a valuable reference for understanding the logical operations performed by the NOR gate within digital circuits.

(iii) The XOR Gate:

The Boolean expression governing the XOR gate is expressed as follows:

$$y = A \cdot \bar{B} + \bar{A} \cdot B$$

This expression can be read as "Y equals A XOR B," where the symbol $\oplus$ denotes the exclusive OR (XOR) operation. The XOR gate produces a true output (1) when the number of true inputs (1) is odd, and it generates a false output (0) when the number of true inputs is even. In other words, the XOR gate outputs true when the inputs A and B differ in their logical states and outputs false when they have the same logical state. This Boolean expression succinctly encapsulates the fundamental logic governing the XOR gate's behavior, making it a key element in digital circuit design.