EXERCISE-I

Solids and Crystals

1. The coordination number of Cu

(A) 1 (B) 6
(C) 8 (D) 12

2. Which one of the following is the weakest kind of bonding in solids

(A) Ionic (B) Metallic
(C) Vander Waals (D) Covalent

3. In a crystal, the atoms are located at the position of

(A) Maximum potential energy
(B) Minimum potential energy
(C) Zero potential energy
(D) Infinite potential energy

4. Crystal structure of NaCl is

(A) Fcc
(B) Bcc
(C) Both of the above
(D) None of the above

5. What is the coordination number of sodium ions in the case of sodium chloride structure

(A) 6 (B) 8
(C) 4 (D) 12

6. The distance between the body centred atom and a corner atom in sodium ($a = 4.225\ \mathring{A}$) is

(A) $3.66\ \mathring{A}$ (B) $3.17\ \mathring{A}$
(C) $2.99\ \mathring{A}$ (D) $2.54\ \mathring{A}$

7. A solid that transmits light in visible region and has a very low melting point possesses

(A) Metallic bonding
(B) Ionic bonding
(C) Covalent bonding
(D) Vander Waal's bonding

8. Atomic radius of *fcc* is

(A) $\frac{a}{2}$ (B) $\frac{a}{2\sqrt{2}}$
(C) $\frac{\sqrt{3}}{4}a$ (D) $\frac{\sqrt{3}}{2}a$

9. A solid reflects incident light and it's electrical conductivity decreases with temperature. The binding in this solids

(A) Ionic (B) Covalent
(C) Metallic (D) Molecular

10. The laptop PC's modern electronic watches and calculators use the following for display

(A) Single crystal
(B) Poly crystal
(C) Liquid crystal
(D) Semiconductors

Semiconductors

11. Electrical conductivity of a semiconductor

(A) Decreases with the rise in its temperature
(B) Increases with the rise in its temperature
(C) Does not change with the rise in its temperature
(D) First increases and then decreases with the rise in its temperature

12. Three semi-conductors are arranged in the increasing order of their energy gap as follows. The correct arrangement is

(A) Tellurium, germanium, silicon
(B) Tellurium, silicon, germanium
(C) Silicon, germanium, tellurium
(D) Silicon, tellurium, germanium

13. When a semiconductor is heated, its resistance
(A) Decreases
(B) Increases
(C) Remains unchanged
(D) Nothing is definite

14. In an insulator, the forbidden energy gap between the valence band and conduction band is of the order of
(A) $1\,\text{MeV}$ (B) $0.1\,\text{MeV}$
(C) $1\,\text{eV}$ (D) $5\,\text{eV}$

15. A *N*-type semiconductor is
(A) Negatively charged
(B) Positively charged
(C) Neutral
(D) None of these

16. The energy band gap of Si is
(A) $0.70\,\text{eV}$
(B) 1.1 *eV*
(C) Between $0.70\,\text{eV}$ to $1.1\,\text{eV}$
(D) 5 *eV*

17. The forbidden energy band gap in conductors, semiconductors and insulators are EG_1, EG_2 and EG_3 respectively. The relation among them is
(A) $EG_1 = EG_2 = EG_3$ (B) $EG_1 < EG_2 < EG_3$
(C) $EG_1 > EG_2 > EG_3$ (D) $EG_1 < EG_2 > EG_3$

18. Which statement is
(A) *N*-type germanium is negatively charged and *P*-type germanium is positively charged
(B) Both *N*-type and *P*-type germanium are neutral
(C) *N*-type germanium is positively charged and *P*-type germanium is negatively charged
(D) Both *N*-type and *P*-type germanium are negatively charged

19. When *Ge* crystals are doped with phosphorus atom, then it becomes
(A) Insulator
(B) *P*-type
(C) *N*-type
(D) Superconductor

20. Let n_P and n_e be the number of holes and conduction electrons respectively in a semiconductor. Then
(A) $n_P > n_e$ in an intrinsic semiconductor
(B) $n_P = n_e$ in an extrinsic semiconductor
(C) $n_P = n_e$ in an intrinsic semiconductor
(D) $n_e > n_P$ in an intrinsic semiconductor

21. The intrinsic semiconductor becomes an insulator at
(A) 0°C (B) −100°C
(C) 300 K (D) 0 K

22. The addition of antimony atoms to a sample of intrinsic germanium transforms it to a material which is
(A) Superconductor
(B) An insulator
(C) *N*-type semiconductor
(D) *P*-type semiconductor

23. Resistance of semiconductor at $0°\text{K}$ is
(A) Zero (B) Infinite
(C) Large (D) Small

24. In a good conductor the energy gap between the conduction band and the valence band is
(A) Infinite (B) Wide
(C) Narrow (D) Zero

25. The impurity atom added to germanium to make it *N*-type semiconductor is
(A) Arsenic (B) Iridium
(C) Aluminium (D) Iodine

26. When *N*-type of semiconductor is heated
(A) Number of electrons increases while that of holes decreases
(B) Number of holes increases while that of electrons decreases
(C) Number of electrons and holes remains same
(D) Number of electrons and holes increases equally

27. To obtain a *P*-type germanium semiconductor, it must be doped with
(A) Arsenic (B) Antimony
(C) Indium (D) Phosphorus

28. The temperature coefficient of resistance of a semiconductor
(A) Is always positive
(B) Is always negative
(C) Is zero
(D) May be positive or negative or zero

29. *P*-type semiconductor is formed when
I. *As* impurity is mixed in *Si*
II. *Al* impurity is mixed in *Si*
III. *B* impurity is mixed in *Ge*
IV. *P* impurity is mixed in *Ge*
(A) I and III (B) I and IV
(C) II and III (D) II and IV

30. In case of a semiconductor, which of the following statement is wrong
(A) Doping increases conductivity
(B) Temperature coefficient of resistance is negative
(C) Resisitivity is in between that of a conductor and insulator
(D) At absolute zero temperature, it behaves like a conductor

31. Which is the correct relation for forbidden energy gap in conductor, semi conductor and insulator
(A) $\Delta Eg_c > \Delta Eg_{sc} > \Delta Eg_{insulator}$
(B) $\Delta Eg_{insulator} > \Delta Eg_{sc} > \Delta Eg_{conductor}$
(C) $\Delta Eg_{conductor} > \Delta Eg_{insulator} > \Delta Eg_{sc}$
(D) $\Delta Eg_{sc} > \Delta Eg_{conductor} > \Delta Eg_{insulator}$

32. The band gap in Germanium and silicon in *eV* respectively is
(A) 0.7, 1.1 (B) 1.1, 0.7
(C) 1.1, 0 (D) 0, 1.1

33. *P*-type semiconductors are made by adding impurity element
(A) *As* (B) *P*
(C) *B* (D) *Bi*

34. At room temperature, a *P*-type semiconductor has
(A) Large number of holes and few electrons
(B) Large number of free electrons and few holes
(C) Equal number of free electrons and holes
(D) No electrons or holes

35. In intrinsic semiconductor at room temperature, number of electrons and holes are
(A) Unequal (B) Equal
(C) Infinite (D) Zero

36. The valence band and conduction band of a solid overlap at low temperature, the solid may be
(A) A metal
(B) A semiconductor
(C) An insulator
(D) None of these

37. Which impurity is doped in *Si* to form *N*-type semi-conductor?
(A) *Al* (B) *B*
(C) *As* (D) None of these

38. In a semiconductor
(A) There are no free electrons at any temperature
(B) The number of free electrons is more than that in a conductor
(C) There are no free electrons at 0 *K*
(D) None of these

39. The energy band gap is maximum in
(A) Metals
(B) Superconductors
(C) Insulators
(D) Semiconductors

40. The process of adding impurities to the pure semiconductor is called
(A) Drouping (B) Drooping
(C) Doping (D) None of these

41. Intrinsic semiconductor is electrically neutral. Extrinsic semiconductor having large number of current carriers would
(A) Positively charged
(B) Negatively charged
(C) Positively charged or negatively charged depending upon the type of impurity that has been added
(D) Electrically neutral

42. If n_e and v_d be the number of electrons and drift velocity in a semiconductor. When the temperature is increased
(A) n_e increases and v_d decreases
(B) n_e decreases and v_d increases
(C) Both n_e and v_d increases
(D) Both n_e and v_d decreases

43. In extrinsic semiconductors
(A) The conduction band and valence band overlap
(B) The gap between conduction band and valence band is more than 16 eV
(C) The gap between conduction band and valence band is near about 1 eV
(D) The gap between conduction band and valence band will be 100 eV and more

44. Resistivity of a semiconductor depends
(A) Shape of semiconductor
(B) Atomic nature of semiconductor
(C) Length of semiconductor
(D) Shape and atomic nature of semiconductor

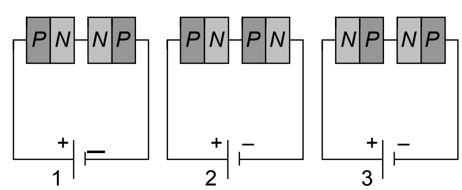
45. Electric current is due to drift of electrons in
(A) Metallic conductors
(B) Semi-conductors
(C) Both (A) and (B)
(D) None of these

Semiconductor Diode

46. The *PN* junction diode is used as
(A) An amplifier (B) A rectifier
(C) An oscillator (D) A modulator

47. When a *PN* junction diode is reverse biased
(A) Electrons and holes are attracted towards each other and move towards the depletion region
(B) Electrons and holes move away from the junction depletion region
(C) Height of the potential barrier decreases
(D) No change in the current takes place

48. Two *PN*-junctions can be connected in series by three different methods as shown in the figure. If the potential difference in the junctions is the same, then the correct connections will be



(A) In the circuit (1) and (2)
(B) In the circuit (2) and (3)
(C) In the circuit (1) and (3)
(D) Only in the circuit (1)

49. A *PN*- junction has a thickness of the order of
(A) 1cm (B) 1mm
(C) 10^{-6} m (D) 10^{-12} cm

50. In the depletion region of an unbiased *P-N* junction diode there are

(A) Only electrons

(B) Only holes

(C) Both electrons and holes

(D) Only fixed ions

51. In a junction diode, the holes are due to

(A) Protons

(B) Neutrons

(C) Extra electrons

(D) Missing of electrons

52. In forward bias, the width of potential barrier in a *P-N* junction diode

(A) Increases

(B) Decreases

(C) Remains constant

(D) First increases then decreases

53. The cause of the potential barrier in a *P-N* diode is

(A) Depletion of positive charges near the junction

(B) Concentration of positive charges near the junction

(C) Depletion of negative charges near the junction

(D) Concentration of positive and negative charges near the junction

54. In a *PN*-junction diode not connected to any circuit

(A) The potential is the same everywhere

(B) The *P*-type is a higher potential than the *N*-type side

(C) There is an electric field at the junction directed from the *N*- type side to the *P*- type side

(D) There is an electric field at the junction directed from the *P*-type side to the *N*-type side

55. Which of the following statements is not true

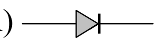
(A) The resistance of intrinsic semiconductors decrease with increase of temperature

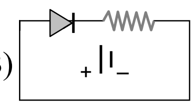
(B) Doping pure *Si* with trivalent impurities give *P*-type semiconductors

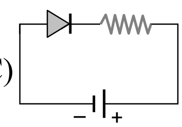
(C) The majority carriers in *N*-type semiconductors are holes

(D) A *PN*-junction can act as a semiconductor diode

56. Which one is in forward bias

(A) 

(B) 

(C) 

(D) None of these

57. The reason of current flow in *P-N* junction in forward bias is

(A) Drifting of charge carriers

(B) Minority charge carriers

(C) Diffusion of charge carriers

(D) All of these

58. The resistance of a reverse biased *P-N* junction diode is about]

(A) 1 *ohm* (B) 10^2 *ohm*

(C) 10^3 *ohm* (D) 10^6 *ohm*

59. Consider the following statements *A* and *B* and identify the correct choice of the given answers

I: The width of the depletion layer in a *P-N* junction diode increases in forwards bias

II: In an intrinsic semiconductor the fermi energy level is exactly in the middle of the forbidden gap

(A) *I* is true and *II* is false

(B) Both *I* and *II* are false

(C) *I* is false and *II* is true

(D) Both *I* and *II* are true

60. In comparison to a half wave rectifier, the full wave rectifier gives lower

(A) Efficiency

(B) Average *dc*

(C) Average output voltage

(D) None of these

61. If no external voltage is applied across *P*-*N* junction, there would be

(A) No electric field across the junction

(B) An electric field pointing from *N*-type to *P*-type side across the junction

(C) An electric field pointing from *P*-type to *N*-type side across the junction

(D) A temporary electric field during formation of *P*-*N* junction that would subsequently disappear

62. In a *PN*-

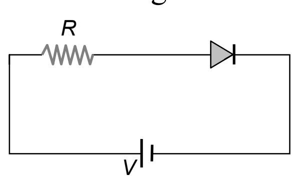
(A) *P* and *N* both are at same potential

(B) High potential at *N* side and low potential at *P* side

(C) High potential at *P* side and low potential at *N* side

(D) Low potential at *N* side and zero potential at *P* side

63. For the given circuit of *PN*-junction diode, which of the following statement is correct



(A) In forward biasing the voltage across *R* is *V*

(B) In forward biasing the voltage across *R* is 2*V*

(C) In reverse biasing the voltage across *R* is *V*

(D) In reverse biasing the voltage across *R* is 2*V*

64. On adjusting the *P*-*N* junction diode in forward biased

(A) Depletion layer increases

(B) Resistance increases

(C) Both decreases

(D) None of these

65. In the middle of the depletion layer of a reverse-biased *PN* junction, the

(A) Potential is zero

(B) Electric field is zero

(C) Potential is maximum

(D) Electric field is maximum

66. Zener breakdown takes place if

(A) Doped impurity is low

(B) Doped impurity is high

(C) Less impurity in *N*-part

(D) Less impurity in *P*-type

67. Consider the following statements *A* and *B* and identify the correct choice of the given answers

I. A zener diode is always connected in reverse bias

II. The potential barrier of a *PN* junction lies between 0.1 to 0.3 *V* approximately

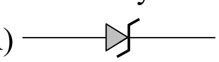
(A) I and II are correct

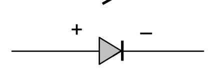
(B) I and II are wrong

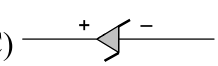
(C) I is correct but II is wrong

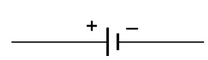
(D) I is wrong but II is correct

68. The correct symbol for zener diode is

(A) 

(B) 

(C) 

(D) 

69. Which one of the following statements is not correct

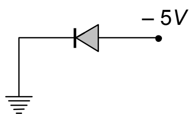
(A) A diode does not obey Ohm's law

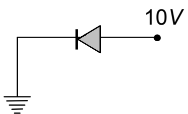
(B) A *PN* junction diode symbol shows an arrow identifying the direction of current (forward) flow

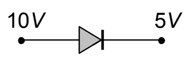
(C) An ideal diode is an open switch

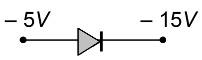
(D) An ideal diode is an ideal one way conductor

70. Which of the following semi-conductor diodes is reverse biased

(A) 

(B) 

(C) 

(D) 

71. No bias is applied to a *P-N* junction, then the current

(A) Is zero because the number of charge carriers flowing on both sides is same

(B) Is zero because the charge carriers do not move

(C) Is non-zero

(D) None of these

72. Zener diode is used as

(A) Half wave rectifier

(B) Full wave rectifier

(C) ac voltage stabilizer

(D) dc voltage stabilizer

73. The width of forbidden gap in silicon crystal is 1.1 *eV*. When the crystal is converted in to a *N*-type semiconductor the distance of Fermi level from conduction band is

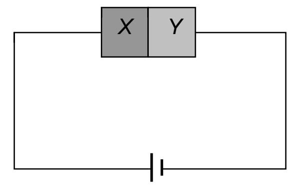
(A) Greater than 0.55 *eV*

(B) Equal to 0.55 *eV*

(C) Lesser than 0.55 *eV*

(D) Equal to 1.1 *eV*

74. A semiconductor *X* is made by doping a germanium crystal with arsenic ($Z = 33$). A second semiconductor *Y* is made by doping germanium with indium ($Z = 49$). The two are joined end to end and connected to a battery as shown. Which of the following statements is correct



(A) *X* is *P*-type, *Y* is *N*-type and the junction is forward biased

(B) *X* is *N*-type, *Y* is *P*-type and the junction is forward biased

(C) *X* is *P*-type, *Y* is *N*-type and the junction is reverse biased

(D) *X* is *N*-type, *Y* is *P*-type and the junction is reverse biased

75. In *P-N* junction, the barrier potential offers resistance]

(A) Free electrons in *N* region and holes in *P* region

(B) Free electrons in *P* region and holes in *N* region

(C) Only free electrons in *N* region

(D) Only holes in *P* region

Junction Transistor

76. In a *PNP* transistor working as a common-base amplifier, current gain is 0.96 and emitter current is 7.2 *mA*. The base current is

(A) 0.4 *mA* (B) 0.2 *mA*

(C) 0.29 *mA* (D) 0.35 *mA*

77. If l_1, l_2, l_3 are the lengths of the emitter, base and collector of a transistor then

(A) $l_1 = l_2 = l_3$ (B) $l_3 < l_2 > l_1$

(C) $l_3 < l_1 < l_2$ (D) $l_3 > l_1 > l_2$

78. In an *NPN* transistor circuit, the collector current is 10 mA. If 90% of the electrons emitted reach the collector, the emitter current (i_E) and base current (i_B) are given by

(A) $i_E = -1\ mA$, $i_B = 9\ mA$

(B) $i_E = 9\ mA$, $i_B = -1\ mA$

(C) $i_E = 1\ mA$, $i_B = 11\ mA$

(D) $i_E = 11\ mA$, $i_B = 1\ mA$

79. In a common emitter transistor, the current gain is 80. What is the change in collector current, when the change in base current is 250 μA

(A) $80 \times 250\ \mu A$ (B) $(250 - 80)\ \mu A$

(C) $(250 + 80)\ \mu A$ (D) $250/80\ \mu A$

80. Least doped region in a

(A) Either emitter or collector

(B) Base

(C) Emitter

(D) Collector

81. For a transistor, the current amplification factor is 0.8. The transistor is connected in common emitter configuration. The change in the collector current when the base current changes by 6 mA is

(A) 6 mA (B) 4.8 mA

(C) 24 mA (D) 8 mA

82. In a common base amplifier circuit, calculate the change in base current if that in the emitter current is 2 mA and $\alpha = 0.98$

(A) 0.04 mA (B) 1.96 mA

(C) 0.98 mA (D) 2 mA

83. In case of *NPN*-transistors the collector current is always less than the emitter current because

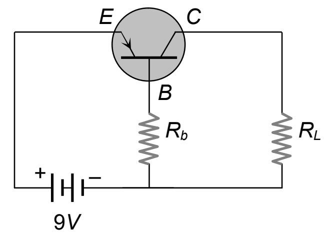
(A) Collector side is reverse biased and emitter side is forward biased

(B) After electrons are lost in the base and only remaining ones reach the collector

(C) Collector side is forward biased and emitter side is reverse biased

(D) Collector being reverse biased attracts less electrons

84. In a transistor circuit shown here the base current is 35 μA. The value of the resistor R_b is



(A) 123.5 $k\Omega$ (B) 257 $k\Omega$

(C) 380.05 $k\Omega$ (D) None of these

85. In a transistor, a change of 8.0mA in the emitter current produces a change of 7.8mA in the collector current. What change in the base current is necessary to produce the same change in the collector current

(A) 50 μA (B) 100 μA

(C) 150 μA (D) 200 μA

86. In a transistor configuration β-parameter is

(A) $\frac{l_b}{l_c}$ (B) $\frac{l_c}{l_b}$

(C) $\frac{l_c}{l_a}$ (D) $\frac{l_a}{l_c}$

87. Which of these is unipolar transistor

(A) Point contact transistor

(B) Field effect transistor

(C) *PNP* transistor

(D) None of these

88. For a transistor, in a common emitter arrangement, the alternating current gain β is given by

(A) $\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_C}$ (B) $\beta = \left(\frac{\Delta I_B}{\Delta I_C}\right)_{V_C}$

(C) $\beta = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_C}$ (D) $\beta = \left(\frac{\Delta I_E}{\Delta I_C}\right)_{V_C}$

89. The relation between α and β parameters of current gains for a transistors is given by

(A) $\alpha = \dfrac{\beta}{1-\beta}$ (B) $\alpha = \dfrac{\beta}{1+\beta}$

(C) $\alpha = \dfrac{1-\beta}{\beta}$ (D) $\alpha = \dfrac{1+\beta}{\beta}$

90. When *NPN* transistor is used as an amplifier

(A) Electrons move from base to emitter

(B) Electrons move from emitter to base

(C) Electrons moves from base to emitter

(D) Holes moves from base to emitter

Digital Electronics

91. A gate has the following truth table

P	1	1	0	0
Q	1	0	1	0
R	1	0	0	0

The gate is

(A) NOR (B) OR

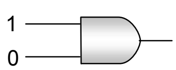
(C) NAND (D) AND

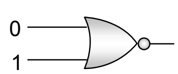
92. How many NAND gates are used to form an AND gate

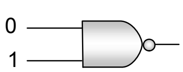
(A) 1 (B) 2

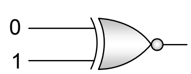
(C) 3 (D) 4

93. Which of the following gates will have an output of 1

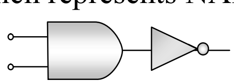
(A) 

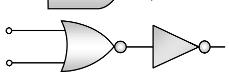
(B) 

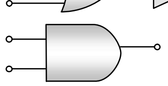
(C) 

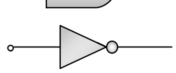
(D) 

94. Which represents NAND gate

(A) 

(B) 

(C) 

(D) 

95. The given truth table is of

A	*X*
0	1
1	0

(A) OR gate (B) AND gate

(C) NOT gate (D) None of above

96. What will be the input of *A* and *B* for the Boolean expression $\overline{(A+B)}\cdot\overline{(A\cdot B)}=1$

(A) 0, 0 (B) 0, 1

(C) 1, 0 (D) 1, 1

97. If *A* and *B* are two inputs in AND gate, then AND gate has an output of 1 when the values of *A* and *B* are

(A) $A = 0, B = 0$ (B) $A = 1, B = 1$

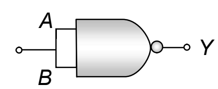
(C) $A = 1, B = 0$ (D) $A = 0, B = 1$

98. The Boolean equation of NOR gate is

(A) $C = A + B$ (B) $C = \overline{A+B}$

(C) $C = A \cdot B$ (D) $C = \overline{A \cdot B}$

99. This symbol represents



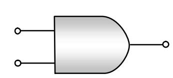
(A) NOT gate

(B) OR gate

(C) AND gate

(D) NOR gate

100. Which logic gate is represented by following diagram

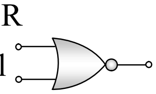


(A) AND

(B) OR

(C) NOR

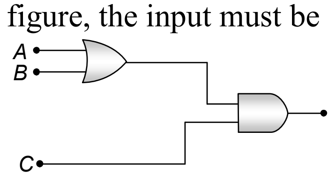
(D) XOR

101. Symbol  represents

(A) NAND gate (B) NOR gate

(C) NOT gate (D) XNOR gate

102. To get an output 1 from the circuit shown in the figure, the input must be



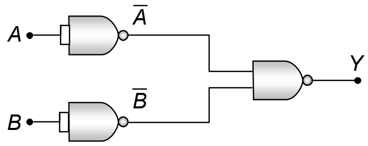
(A) A = 0, B = 1, C = 0

(B) A = 1, B = 0, C = 0

(C) A = 1, B = 0, C = 1

(D) A = 1, B = 1, C = 0

103. The combination of the gates shown in the figure below produces



(A) NOR gate
(B) OR gate
(C) AND gate
(D) XOR gate

104. The output of a NAND gate is 0
(A) If both inputs are 0
(B) If one input is 0 and the other input is 1
(C) If both inputs are 1
(D) Either if both inputs are 1 or if one of the inputs is 1 and the other 0

105. A gate in which all the inputs must be low to get a high output is called
(A) A NAND gate (B) An inverter
(C) A NOR gate (D) An AND gate

Valve Electronics (Diode and Triode)

106. In a triode amplifier, $\mu = 25, r_p = 40$ kilo ohm and load resistance $R_L = 10$ kilo ohm. If the input signal voltage is 0.5 volt, then output signal voltage will be
(A) 1.25 *volt* (B) 5 *volt*
(C) 2.5 *volt* (D) 10 *volt*

107. The amplification factor of a triode is 20. If the grid potential is reduced by 0.2 *volt* then to keep the plate current constant its plate voltage is to be increased by
(A) 10 *volt* (B) 4 *volt*
(C) 40 *volt* (D) 100 *volt*

108. For a triode $r_p = 10$ *kilo ohm* and $g_m = 3$ *milli mho*. If the load resistance is double of plate resistance, then the value of voltage gain will be
(A) 10 (B) 20
(C) 15 (D) 30

109. The amplification produced by a triode is due to the action of
(A) Filament (B) Cathode
(C) Grid (D) Plate

110. In an experiment, the saturation in the plate current in a diode is observed at 240*V*. But a student still wants to increase the plate current. It can be done, if
(A) The plate voltage is increased further
(B) The plate voltage is decreased
(C) The filament current is decreased
(D) The filament current is increased

111. In a triode amplifier, the value of maximum gain is equal to
(A) Half the amplification factor
(B) Amplification factor
(C) Twice the amplification factor
(D) Infinity

112. For a given triode $\mu = 20$. The load resistance is 1.5 times the anode resistance. The maximum gain will
(A) 16
(B) 12
(C) 10
(D) None of the above

113. The voltage gain of a triode depends upon
(A) Filament voltage (B) Plate voltage
(C) Plate resistance (D) Plate current

114. In a triode valve
(A) If the grid voltage is zero then plate current will be zero
(B) If the temperature of filament is doubled, then the thermionic current will also be doubled
(C) If the temperature of filament is doubled, then the thermionic current will nearly be four times
(D) At a definite grid voltage the plate current varies with plate voltage according to Ohm's law

115. The amplification factor of a triode valve is 15. If the grid voltage is changed by 0.3 *volt* the change in plate voltage in order to keep the plate current constant (in volt)]

(A) 0.02 (B) 0.002
(C) 4.5 (D) 5.0

116. The slope of plate characteristic of a vacuum tube diode for certain operating point on the curve is $10^{-3}\frac{\text{mA}}{\text{V}}$. The plate resistance of the diode and its nature respectively

(A) 100 kilo-ohms static
(B) 1000 *kilo-ohms* static
(C) 1000 *kilo-ohms* dynamic
(D) 100 *kilo-ohms* dynamic

117. A triode has a mutual conductance of 2×10^{-3} mho and an amplification factor of 50. The anode is connected through a resistance of 25×10^{3} *ohms* to a 250 *volts* supply. The voltage gain of this amplifier is

(A) 50 (B) 25
(C) 100 (D) 12.5

118. 14×10^{15} electrons reach the anode per second. If the power consumed is 448 *milliwatts*, then the plate (anode) voltage is

(A) 150 *V* (B) 200*V*
(C) 14×448V (D) 448/14*V*

119. In the circuit of a triode valve, there is no change in the plate current, when the plate potential is increased from 200 *volt* to 220 *volt* and the grid potential is decreased from –0.5 *volt* to –1.3 *volt*. The amplification factor of this valve is

(A) 15 (B) 20
(C) 25 (D) 35

120. If the amplification factor of a triode (μ) is 22 and its plate resistance is 6600 *ohm*, then the mutual conductance of this valve is mho is

(A) $\frac{1}{300}$ (B) 25×10^{-2}
(C) 2.5×10^{-2} (D) 0.25×10^{-2}

121. Diode is used as a/an

(A) Oscillator (B) Amplifier
(C) Rectifier (D) Modulator

122. The electrical circuits used to get smooth d.c. output from a rectifier circuit is called

(A) Filter (B) Amplifier
(C) Full wave rectifier (D) Oscillator

123. Which of the following does not vary with plate or grid voltages

(A) g_m
(B) R_p
(C) μ
(D) Each of them varies

124. The grid in a triode valve is

(A) To increases the thermionic emission
(B) To control the plate to cathode current
(C) To reduce the inter-electrode capacity
(D) To keep cathode at constant potential

125. In a triode valve the amplification factor is 20 and mutual conductance is 10^{-3} *mho*. The plate resistance is

(A) $2\times10^{3}\ \Omega$ (B) $4\times10^{3}\ \Omega$
(C) $2\times10^{4}\ \Omega$ (D) $2\times10^{4}\ \Omega$

126. The thermionic emission of electron is due to

(A) Electromagnetic field
(B) Electrostatic field
(C) High temperature
(D) Photoelectric effect

127. The amplification factor of a triode is 50. If the grid potential is decreased by 0.20 *V*, what increase in plate potential will keep the plate current

(A) 5 *V* (B) 10 *V*

(C) 0.2 *V* (D) 50 *V*

128. The slope of plate characteristic of a vacuum diode is 2×10^{-2} mA / V. The plate resistance of diode will be

(A) 50 Ω (B) 50 *k*Ω

(C) 500 *k*Ω (D) 500 *k*Ω

129. The transconductance of a triode amplifier is 2.5 *mili mho* having plate resistance of 20 *K*Ω, amplification 10. Find the load resistance

(A) 5 *k*Ω (B) 25 *k*Ω

(C) 20 *k*Ω (D) 50 *k*Ω

130. The amplification factor of a triode is 18 and its plate resistance is $8 \times 10^3 \Omega$. A load resistance of $10^4 \Omega$ is connected in the plate circuit. The voltage gain will be

(A) 30 (B) 20

(C) 10 (D) 1